DIPLOMA 4TH SEM EE
ANALOG ELECTRONICS & OP-AMP

CHAPTER-1

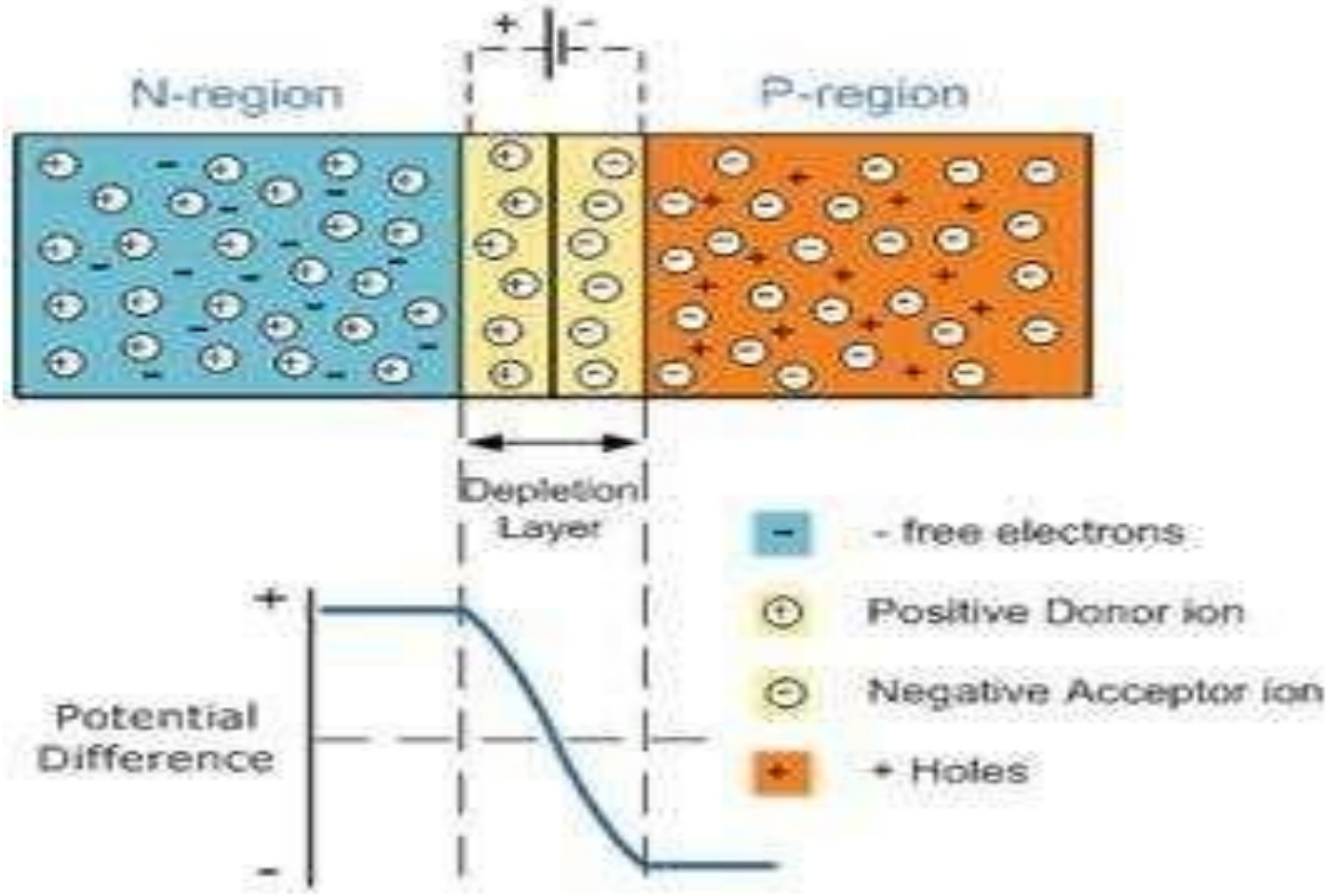
P-N JUNCTION DIODE

PN JUNCTION DIODE

- *When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called* ***pn junction***
- At the instant of *pn-junction formation, the free electrons near the junction in the n region begin to* diffuse across the junction into the *p region where they combine with holes near the junction.*
- The result is that *n region loses free electrons as they diffuse into the junction. This creates a layer of* positive charges (pentavalent ions) near the junction.

•As the electrons move across the junction, the *p* region loses holes as the electrons and holes combine.
•The result is that there is a layer of negative charges (trivalent ions) near the junction.
•These two layers of positive and negative charges form the
depletion region (or depletion layer).
•*The term depletion is due to the fact that near the junction,*
•The region is depleted (*i.e. emptied) of charge carries (free electrons and holes) due to diffusion across* the junction.
•It may be noted that depletion layer is formed very quickly and is very thin compared to the *n region and the p region.*

PN junction diode digram



•Once *pn junction is formed and depletion layer created, the diffusion of free electrons stops.*

• In other words, the depletion region acts as a barrier to the further movement of free electrons across the junction.

The positive and negative charges set up an electric field. The electric field is a barrier to the free electrons in the *n-region. There exists a potential* difference across the depletion layer and is called **barrier potential (*V0).***

•***The barrier potential of a pn***junction depends upon several factors including the type of semiconductor material, the amount ofdoping and temperature. The typical barrier potential is approximately:

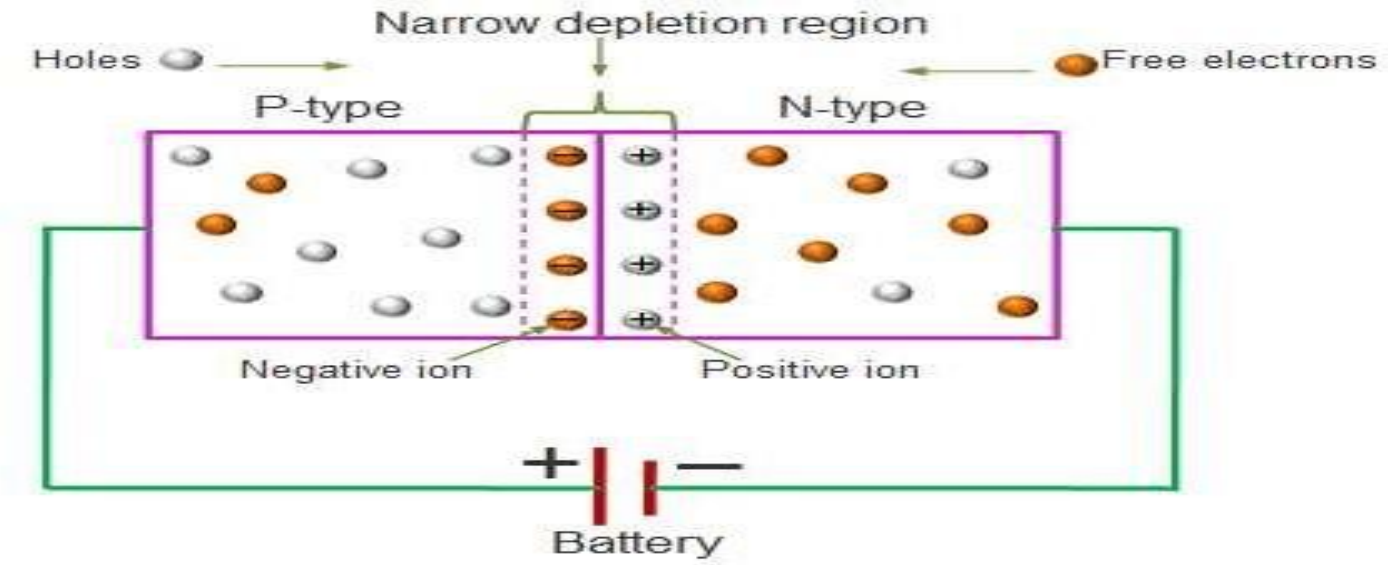
For silicon, *V0 = 0.7 V ; For germanium, V0 = 0.3 V*

Biasing a pn Junction

There are following two bias conditions :

1. Forward biasing 2. Reverse biasing

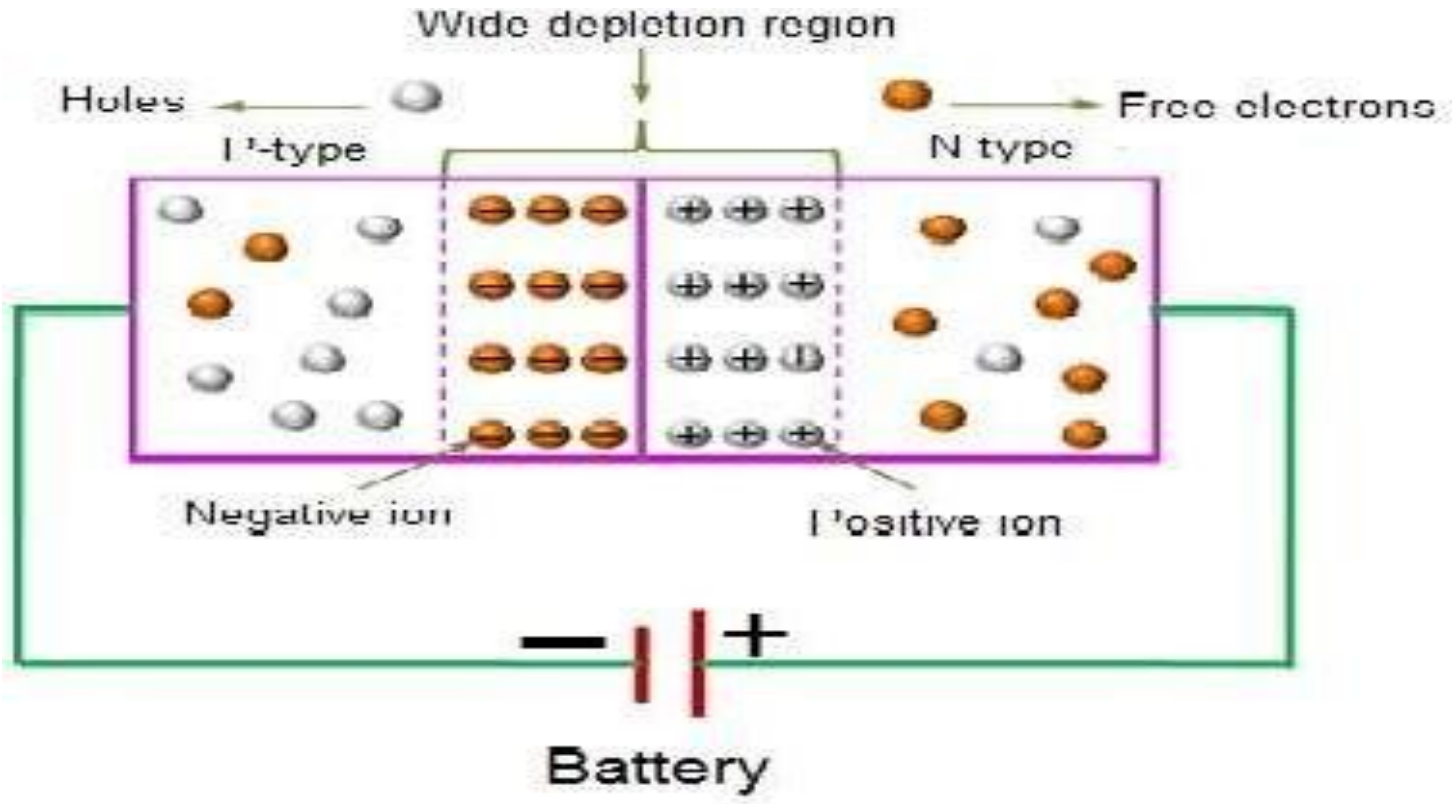
Forward biasing- *When external d.c. voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called* ***forward biasing.***



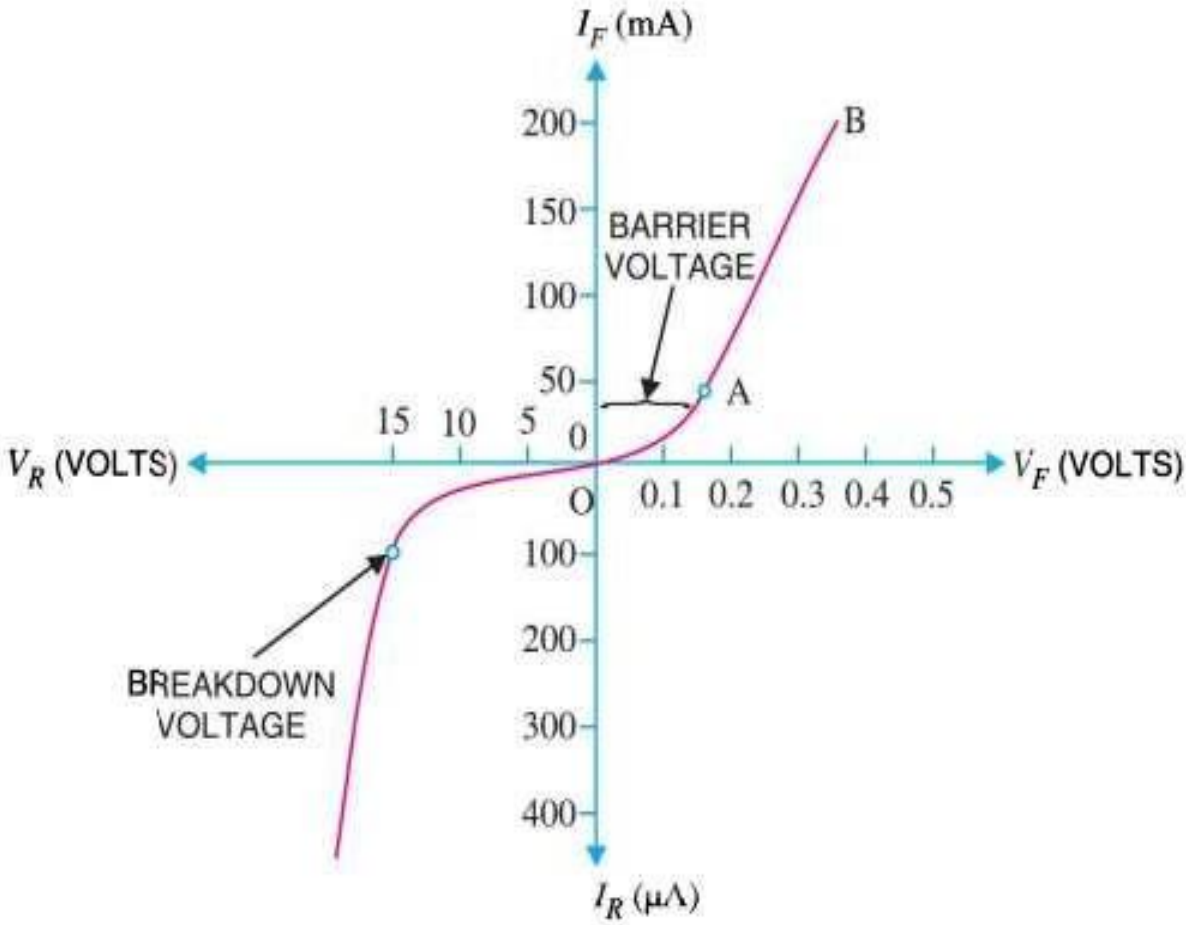
Forward bias

Reverse biasing-

When the external d.c. voltage applied to the junction is in such a *direction that potential barrier is increased, it is called* ***reverse biasing.***



Characteristics of PN Junction Diode



The characteristics can be explained under three cases , such as :

1. **Zero bias, 2.Forward bias , 3.Reverse bias**

- **<u>Zero Bias</u>**
- In zero bias condition , no external voltage is applied to the pn junction .
- Hence, the potential barrier at the junction does not permit current flow.
- Therefore, the circuit current is zero at V=0 V, as indicated by point O in figure below.

Forward Bias

•In forward biased condition , p-type of the pn junction is connected to the positive terminal and n-type is connected to the negative terminal of the external voltage.
This results in reduced potential barrier.

•At some forward voltage i.e 0.7 V for Si and 0.3 V for Ge, the potential barrier is almost eliminated and the current starts flowing in the circuit.

•Form this instant, the current increases with the increase in forward voltage. Hence. a curve OB is obtained with forward bias as shown in figure above.

•From the forward characteristics, it can be noted that at first i.e. region OA , the current increases very slowly and the curve is non-linear. It is because in this region the external voltage applied to the pn junction is used in overcoming the potential barrier.

However, once the external voltage exceeds the potential barrier voltage, the potential barrier is eliminated and the pn junction behaves as an ordinary conductor. Hence , the curve AB rises very sharply with the increase in external voltage and the curve is almost linear.

Reverse Bias

In reverse bias condition , the p-type of the pn junction is connected to the negative terminal and n-type is connected to the positive terminal of the external voltage.
This results in increased potential barrier at the junction. Hence, the junction resistance becomes very high and as a result practically no current flows through the circuit.
However, a very small current of the order of μA , flows through the circuit in practice. This is knows as reverse saturation current(I_S) and it is due to the minority carriers in the junction.

•As we already know, there are few free electrons in p-type material and few holes in n-type material. These free electrons in p-type and holes in n-type are called minority carriers The reverse bias applied to the pn junction acts as forward bias to there minority carriers and hence, small current flows in the reverse direction.

•If the applied reverse voltage is increased continuously, the kinetic energy of the minority carriers may become high enough to knock out electrons from the semiconductor atom.

•At this stage breakdown of the junction may occur. This is characterized by a sudden increase of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

Some imporatant terms

1. **Knee voltage.** *It is the forward voltage at which the current through the junction starts to increase rapidly.*

- When a diode is forward biased, it conducts current very slowly until we overcome the potentialbarrier.
- For silicon *pn junction, potential barrier is 0.7 V whereas it is 0.3 V for germanium junction.*
- It is clear that knee voltage for silicon diode is 0.7 V and 0.3 V for germanium diode.
- Once the applied forward voltage exceeds the knee voltage, the current starts increasing rapidly.

2. **Breakdown voltage.** *It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.*

3. ***Maximum forward current****. It is the highest instantaneous forward current that a pn* junction can conduct without damage to the junction.

•Manufacturer's data sheet usually specifies this rating. If the forward current in a *pn junction is more than this rating, the junction will be destroyed* due to overheating.

4. ***Peak inverse voltage (PIV).*** *It is the maximum reverse voltage that can be applied to the pn* junction without damage to the junction.

•If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat.

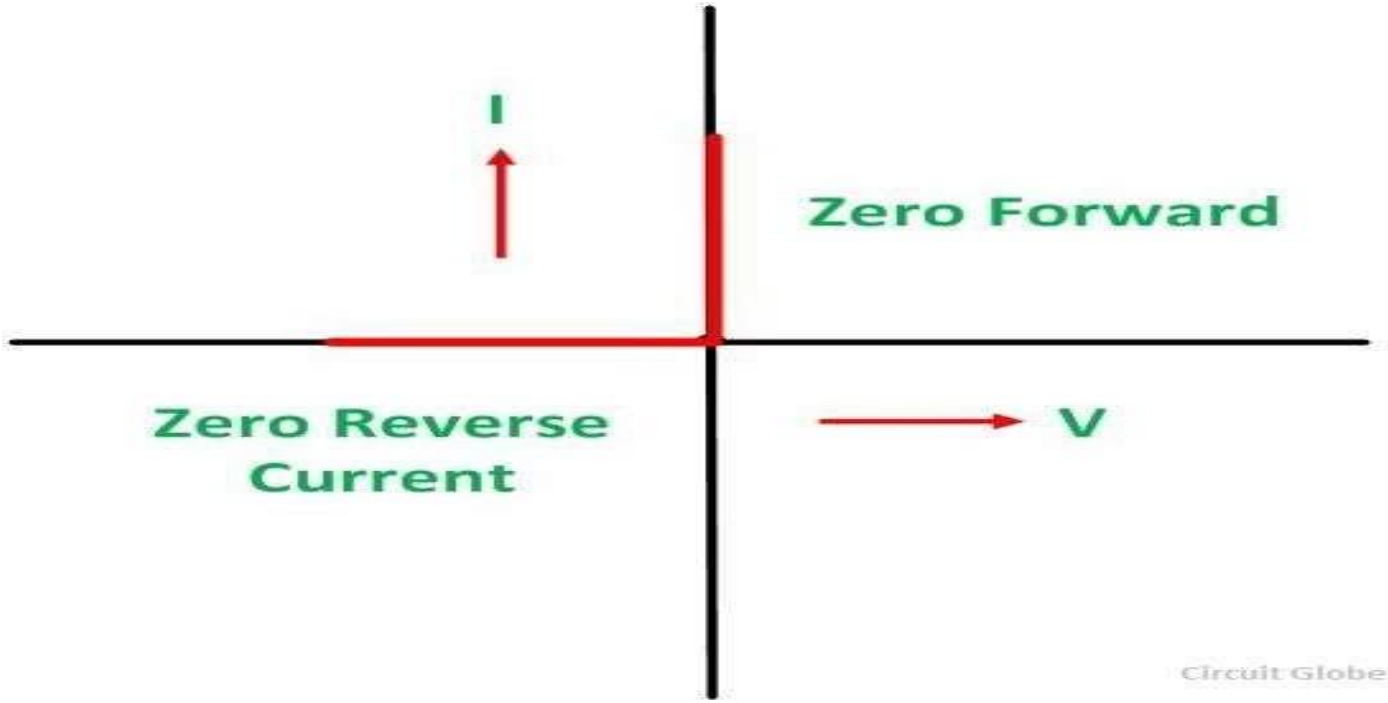
•A *pn junction i.e. a crystal diode is used as a rectifier to change alternating* current into direct current. In such applications, care should be taken that reverse voltage across thediode during negative half-cycle of a.c. does not exceed the PIV of diode.

5.<u>Maximum power rating</u>. *It is the maximum power that can be dissipated at the junction* without damaging it.

•The power dissipated at the junction is equal to the product of junction current and the voltage across the junction.

Ideal Diode

A diode is said to be an **Ideal Diode** when it is forward biased and acts as a perfect conductor, with zero voltage across it. Similarly, when the diode is reversed biased, it acts as a perfect insulator with zero current through it.



Zener breakdown :

The phenomenon of the Zener breakdown occurs in the very thin depletion region. The thin depletion region has more numbers of free electrons. The reverse bias applies across the PN junction develops the electric field intensity across the depletion region. The strength of the electric field intensity becomes very high.

The electric field intensity increases the kinetic energy of the free charge carriers. Thereby the carriers start jumping from one region to another. These energetic charge carriers collide with the atoms of the p-type and n-type material and produce the electron-hole pairs.

The reverse current starts flowing in the junction because of which depletion region entirely vanishes. This process is known as the Zener breakdown.

Avalanche Breakdown

The mechanism of avalanche breakdown occurs because of the reverse saturation current.

The P and N-type materials of the PN junction are not perfect, and they have some impurities in it, i.e., the p-type material has some electrons, and the N-type material has some hole in it. The width of the depletion region varies. Their width depends on the bias applied to the terminal of the P and N region.

The reverse bias increases the electrical field across the depletion region. When the high electric field exists across the depletion, the velocity of minority charge carrier crossing the depletion region increases. These carriers collide with the atoms of the crystal. Because of the violent collision, the charge carrier takes out the electrons from the atom.

The collision increases the electron-hole pair. As the electron-hole induces in the high electric field, they are quickly separated and collide with the other atoms of the crystals. The process is continuous, and the electric field becomes so much higher then the reverse current starts flowing in the PN junction. The process is known as the **Avalanche breakdown**. After the breakdown, the junction cannot regain its original position because the diode is completely burnt off.

CHAPTER-2

SPECIAL SEMICONDUCTOR DEVICES

Thermistor

- A type of resistor whose resistance value is sensitive to the change in temperature is known as Thermistor.
- This is the passive component in the circuit. Material used in construction of this differs from RTD's.
- Resistance Temperature Detectors are popularly known as RTD's and Thermistor.The thermistors are made by using Ceramic or polymers.
- The temperature measured from this thermistor produces accurate values.
- These are of cheap and robust nature. But it doesn't go well when we connect it in extreme cold and hot conditions

sensor

- A **sensor** is a device that responds to some type of the input from the environment such as heat, light, motion, temperature, pressure and moisture.
- It is a device that converts signals from one energy domain to electrical domain.
- The simplest example of a sensor is an LDR or a Light Dependent Resistor. It is a device, whose resistance varies according to intensity of light it is subjected to. When the light falling on an LDR is more, its resistance becomes very less and when the light is less, well, the resistance of the LDR becomes very high.
- We can connect this LDR in a voltage divider (along with other resistor) and check the voltage drop across the LDR. This voltage can be calibrated to the amount of light falling on the LDR.

Zener diode

A properly doped crystal diode which has asharp breakdown voltage is known as a ***zener*** **diode.**

- Below Fig. shows the symbol of a zener diode.
- It may be seen that it is just like an ordinary
- diode except that the bar is turned into *z-shape.*

The following points about the zener diode:

(i) *A zener diode is like an ordinary diode except* that it is properly doped so as to have a sharp breakdown voltage.

(ii) *A zener diode is always reverse connected i.e. it is always reverse biased.*

(iii) *A zener diode has sharp breakdown voltage,*called zener voltage *VZ.*

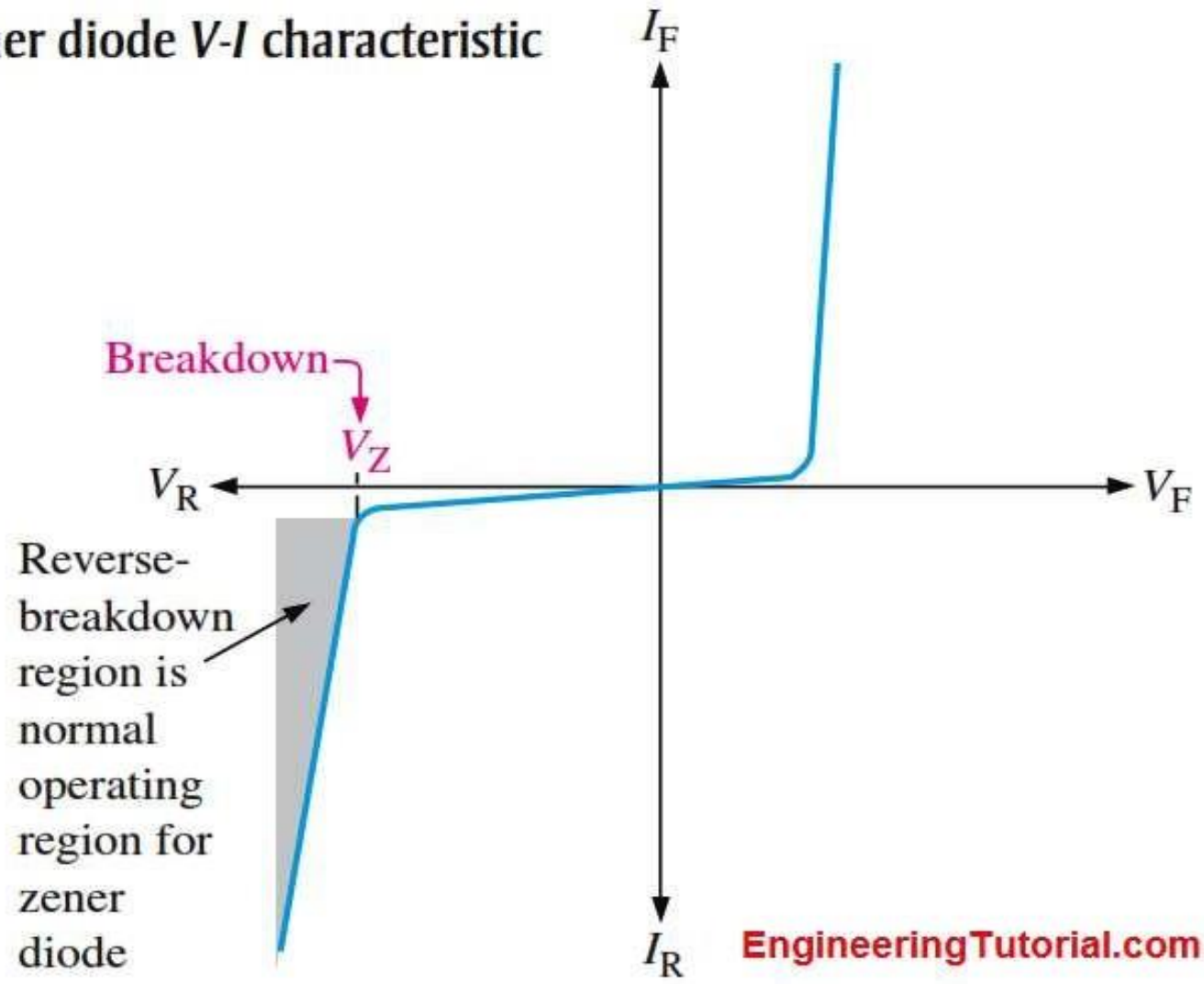
(iv) *When forward biased, its characteristics are just those of ordinary diode.*

(v) *The zener diode is not immediately burnt just because it has entered*

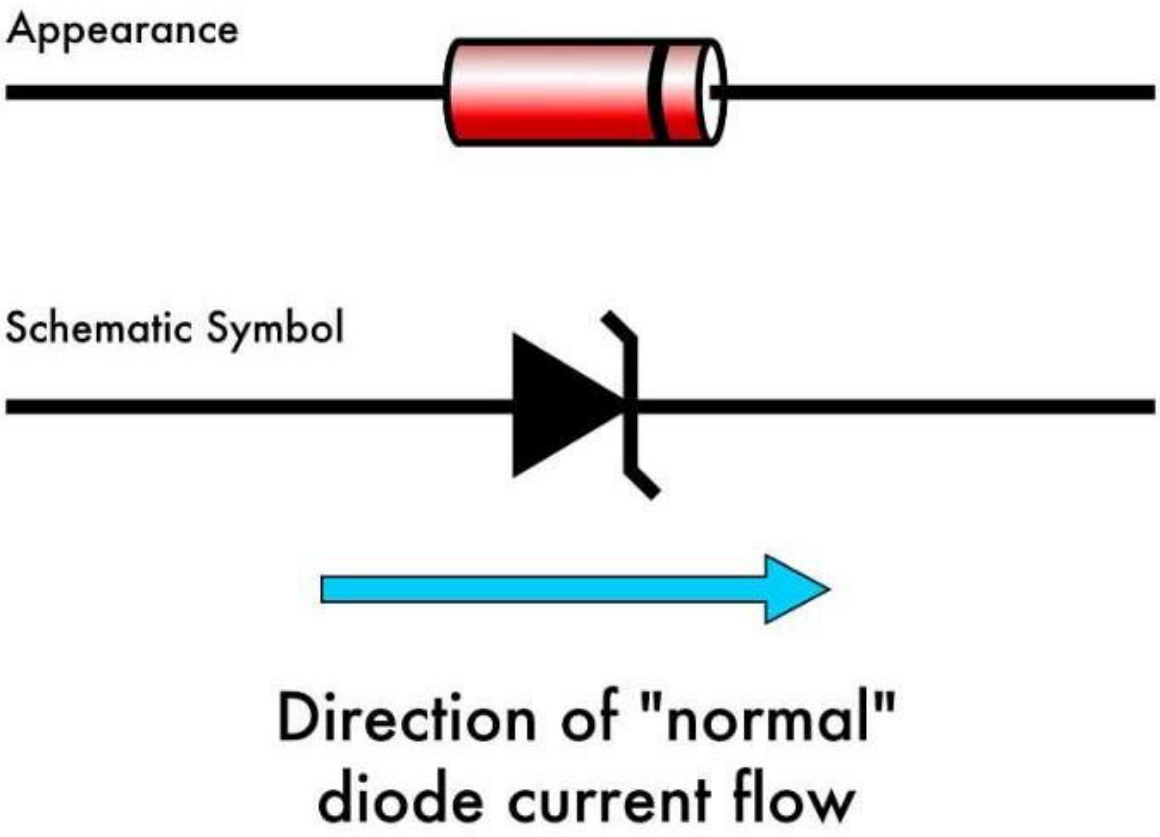
the *breakdown region. As long as the external circuit connected to the diode

limits the diode current to less than *burn out value, the diode will not burnout.*

zener diode *V-I* characteristic



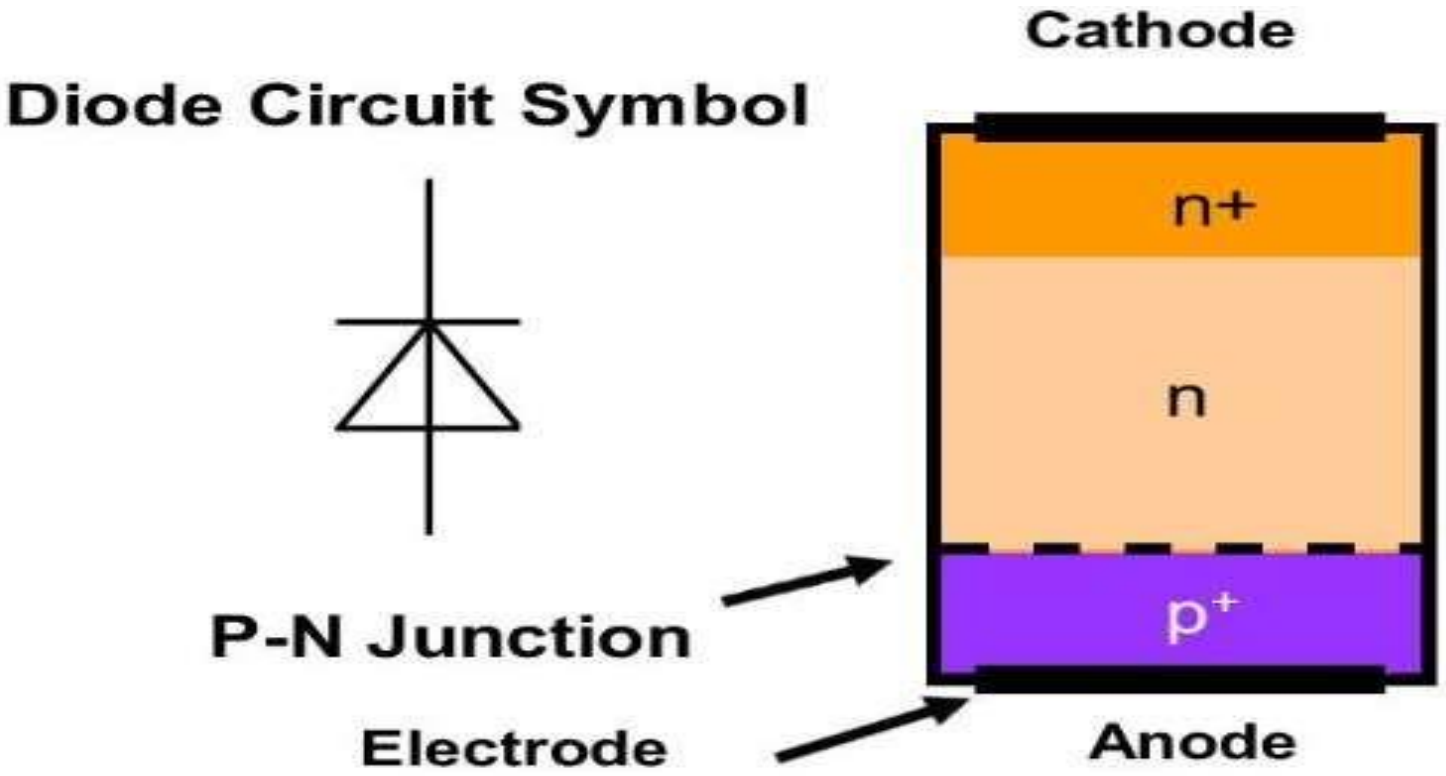
SYMBOL OF ZENER DIODE



PIN DIODE

- The PIN diode is a one type of photo detector, used to convert optical signal into an electrical signal. The PIN diode comprises of three regions, namely P-region, I-region and N-region. Typically, both the P and N regions are heavily doped .
- The intrinsic region in the diode is in contrast to a PN junction diode. The layer between the P & N regions includes no charge carriers as any electrons or holes merge As the depletion region of the diode has no charge carriers it works as an insulator. The depletion region exists within a PIN diode, but if the PIN diode is forward biased, then the carriers come into the depletion region and as the two carrier types get together, the flow of current will starts.
- This region makes the PIN diode an lower rectifier, but it makes it appropriate for fast switches, attenuators, photo detectors and applications of high voltage power electronics.

Structure of PIN Diode

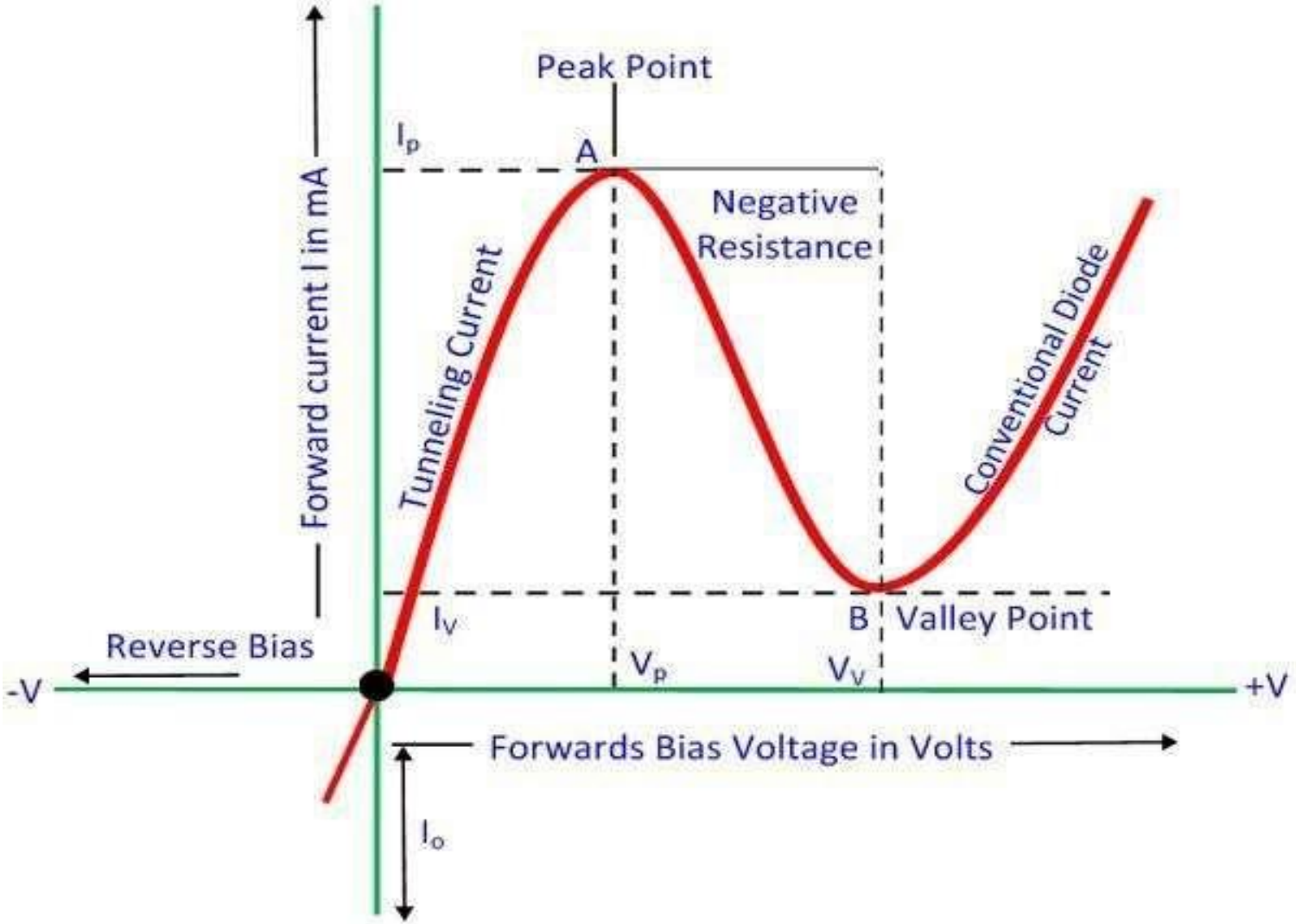


Tunnel Diode

- *A **tunnel diode is a pn junction that exhibits negative resistance between two values of forward**voltage (i.e., between peak-point voltage and valley-point voltage).*
- **Theory. The tunnel diode is basically a *pn junction with heavy doping of p-type and n-type***semiconductor materials. In fact, a tunnel diode is doped approximately 1000 times as heavily as aconventional diode. This heavy doping results in a large number of majority carriers.
- **Tunneling effect-***The movement of valence electrons from the valence energy band to the conduction band withlittle or no applied forward voltage is called **tunneling. Valence electrons seem to tunnel through**the forbidden energy band.*

V-I Characteristic of tunnel

- (***i) As the forward voltage across the tunnel diode is increased from zero, electrons from the nregion***“tunnel” through the potential barrier to the *p-region. As the forward voltage increases, the* diode current also increases until the *peak-point P is reached.*
- *The diode current has now reached* peak current *IP (= 2.2 mA) at about peak-point voltage VP (= 0.07 V). Until now the diode has* exhibited positive resistance.
- (***ii) As the voltage is increased beyond VP, the tunneling action starts decreasing and the diode*** current decreases as the forward voltage is increased until *valley-point V is reached at valley-point*voltage *VV (= 0.7V). In the region between peak-point and valley-point (i.e., between points P andV), the diode exhibits negative* resistance.



V-I Characteristic of Tunnel Diode

(***iii) When forward bias is increased beyond valley-point voltage VV (= 0.7 V), the tunnel diode***behaves as a normal diode. In other words, from point V onwards, the diode current increases withthe increase in forward voltage *i.e., the diode exhibits positive resistance once again. Above Fig.* shows the symbol of tunnel diode. It may be noted that a tunnel diode has a high reverse current but operation under this condition is not generally used.

CHAPTER-3

RECTIFIER CIRCUIT AND FILTERS

Rectifier

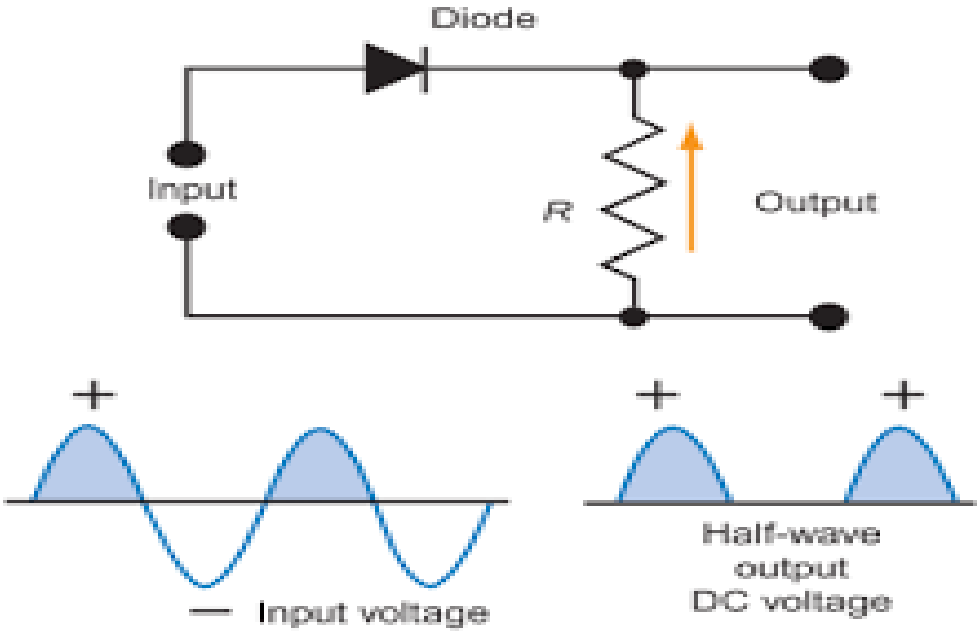
A **rectifier** is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction.

The following two rectifier circuits can be used :

i.Half-wave rectifier *(ii)* Full-wave rectifier

Half-Wave Rect ifier

In half-wave rectification, the rectifier conducts current only during the positive half-cycles of input a.c. supply. The negative half-cycles of a.c. supply are suppressed *i.e.* during negative half-cycles, no current is conducted and hence no voltage appears across the load. Therefore, current always flows in one direction (*i.e.* d.c.) through the load though after every half-cycle



Operation. The a.c. voltage across the secondary winding AB changes polarities after every half-cycle. During the positive half-cycle of input a.c. voltage, end A becomes positive *w.r.t.* end B. This makes the diode forward biased and hence it conducts current. During the negative half-cycle, end A is negative *w.r.t.* end B. Under this condition, the diode is reverse biased and it conducts no current. Therefore, current flows through the diode during positive half-cycles of input a.c. voltage only ; it is blocked during the negative half-cycles . In this way, current flows through load R_L always in the same direction. Hence d.c. output is obtained across R_L. It may be noted that output across the load is pulsating d.c. These pulsations in the output are further smoothened with the help of *filter circuits* discussed later.

Disadvantages : The main disadvantages of a half-wave rectifier are :

(*i*) The pulsating current in the load contains alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.

(*ii*) The a.c. supply delivers power only half the time. Therefore, the output is low.

Efficiency of Half-Wave Rect ifier; *The ratio of d.c. power output to the applied input a.c. power is known as* **rectifier efficiency** *i.e.*

Rectifier efficiency = d.c. power output/ Input a.c. power

Max. rectifier efficiency = 40.6%

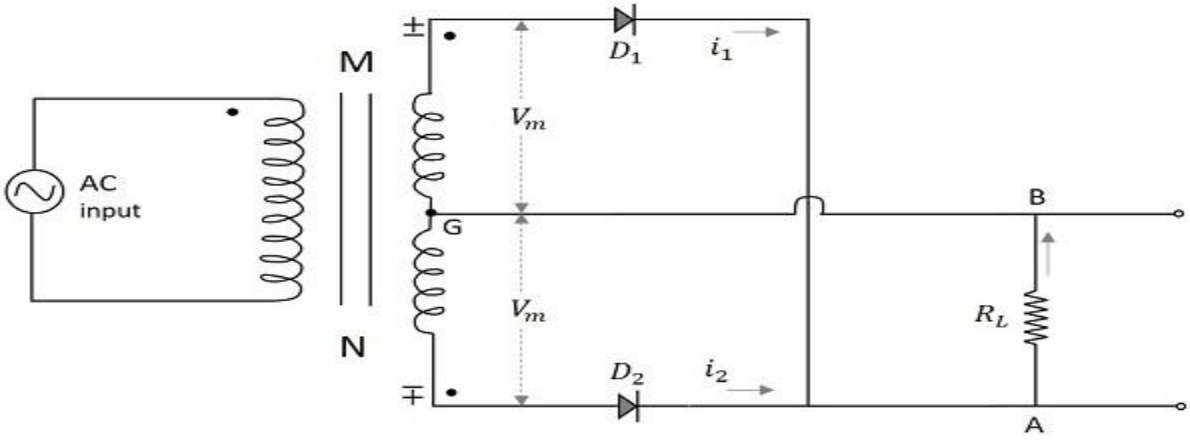
Full-Wave Rectifier

In full-wave rectification, current flows through the load in the same direction for both half-cycles of input a.c. voltage. This can be achieved with two diodes working alternately. For the positive halfcycle of input voltage, one diode supplies current to the load and for the negative half-cycle, the other diode does so ; current being always in the same direction through the load. Therefore, a full-wave rectifier utilises both half-cycles of input a.c. voltage to produce the d.c. output. The following two circuits are commonly used for full-wave rectification :
i) Centre-tap full-wave rectifier ii) Full-wave bridge rectifier

Center-tapped Full-Wave Rectifier-

The features of a center-tapping transformer are −

- The tapping is done by drawing a lead at the mid-point on the secondary winding. This winding is split into two equal halves by doing so.
- The voltage at the tapped mid-point is zero. This forms a neutral point.
- The center tapping provides two separate output voltages which are equal in magnitude but opposite in polarity to each other.



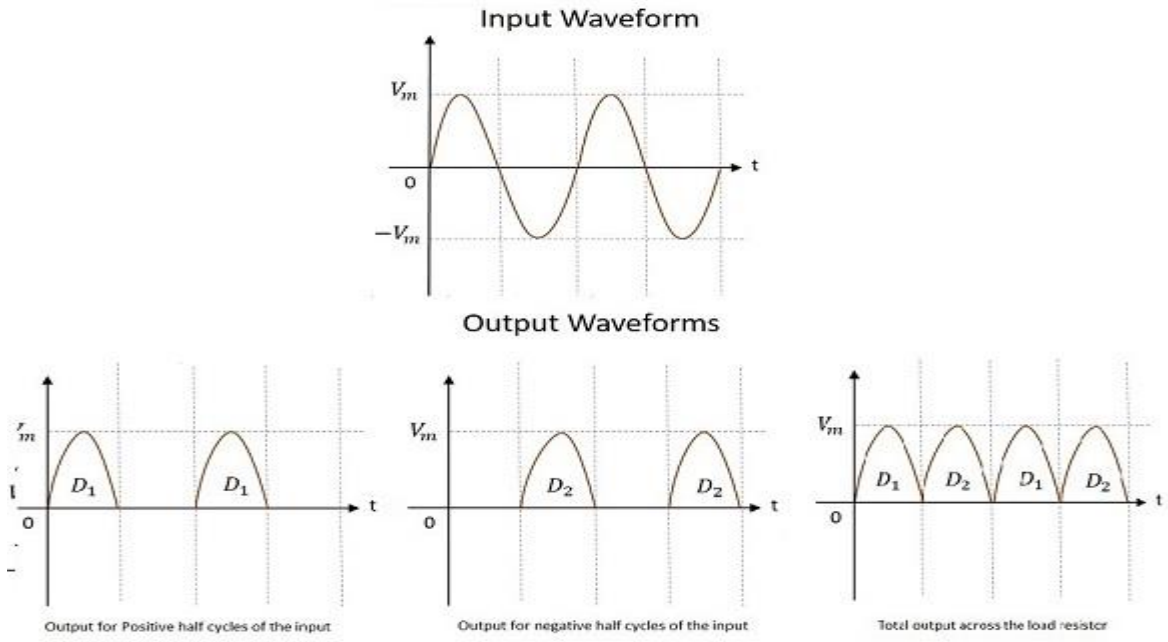
Circuit diagram of a center-tapped full wave rectifier

working of a CT- FWR

The working of a center-tapped full wave rectifier can be understood by the above figure. When the positive half cycle of the input voltage is applied, the point M at the transformer secondary becomes positive with respect to the point N. This makes the diode D_1 forward biased. Hence current i_1 flows through the load resistor from A to B. We now have the positive half cycles in the output.

When the negative half cycle of the input voltage is applied, the point M at the transformer secondary becomes negative with respect to the point N. This makes the diode D_2 forward biased. Hence current i_2

flows through the load resistor from A to B. We now have the positive half cycles in the output, even during the negative half cycles of the input.



Peak Inverse Voltage

As the maximum voltage across half secondary winding is V_m, the whole of the secondary voltage appears across the non-conducting diode. Hence the **peak inverse voltage** is twice the maximum voltage across the half-secondary winding, i.e.

$$PIV=2V_m$$

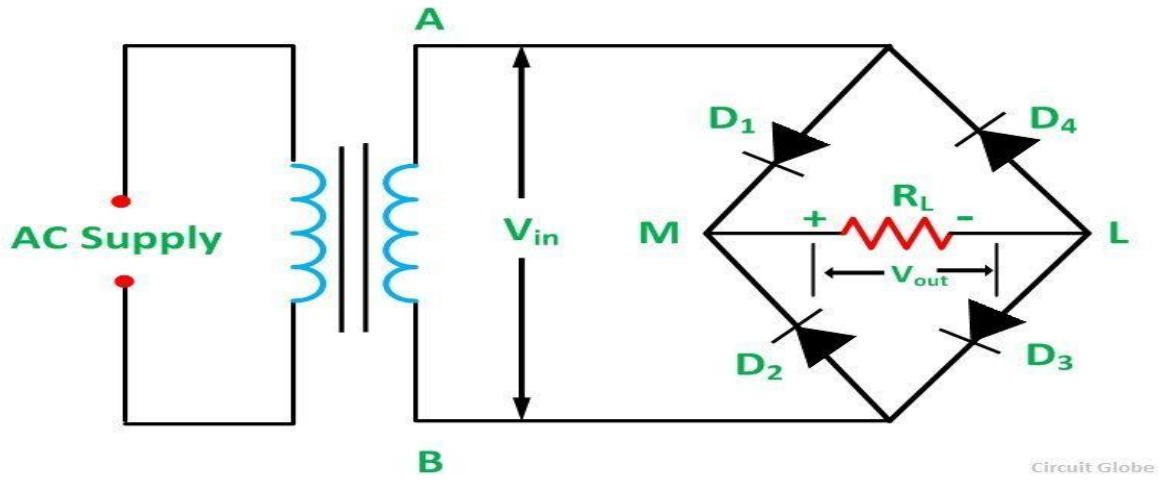
Disadvantages

There are few disadvantages for a center-tapped full wave rectifier such as −

- Location of center-tapping is difficult
- The dc output voltage is small
- PIV of the diodes should be high

Full Wave Bridge Rectifier

In **Full Wave Bridge Rectifier**, an ordinary transformer is used in place of a center-tapped transformer. The circuit forms a bridge connecting the four diodes D_1, D_2, D_3, and D_4. The circuit diagram of the Full Wave Bridge Rectifier is shown below.

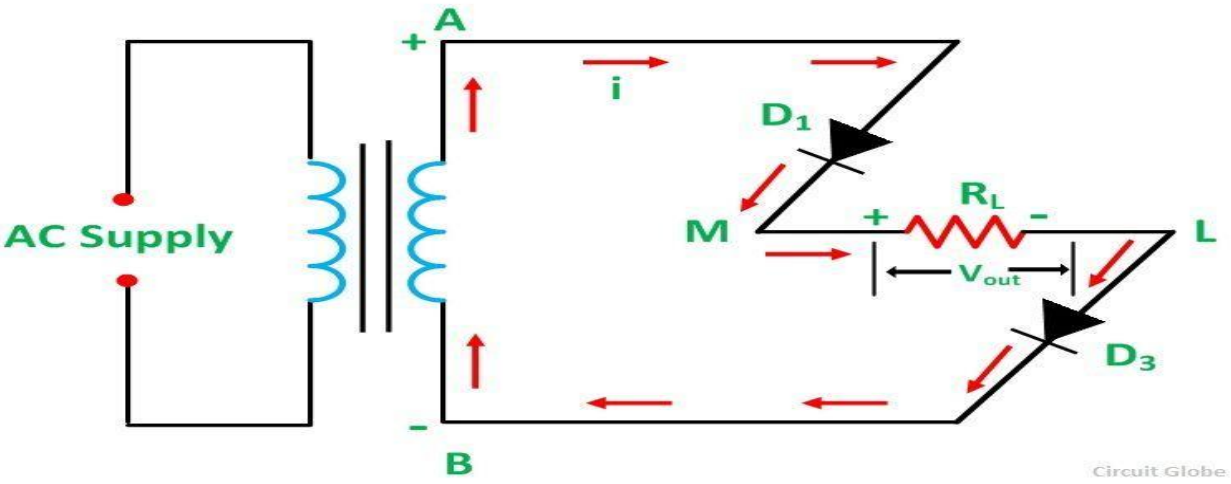


The AC supply which is to be rectified is applied diagonally to the opposite ends of the bridge. Whereas, the load resistor R_L is connected across the remaining two diagonals of the opposite ends of the bridge.

Operation of Full Wave Bridge Rectifier

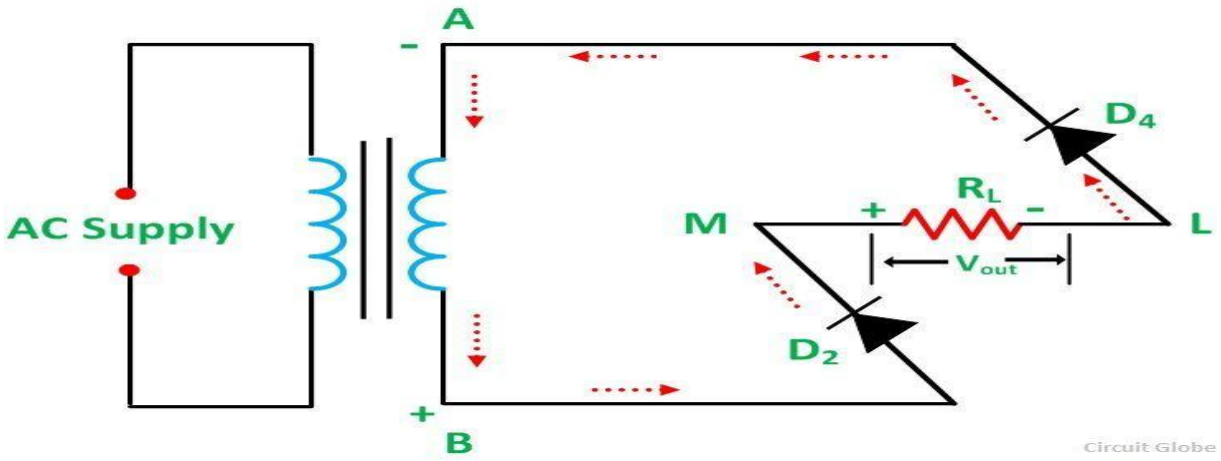
When an AC supply is switched ON, the alternating voltage V_{in} appears across the terminals AB of the secondary winding of the transformer which needs rectification. During the positive half cycle of the secondary voltage, end A becomes positive, and end B becomes negative as shown in the figure below.

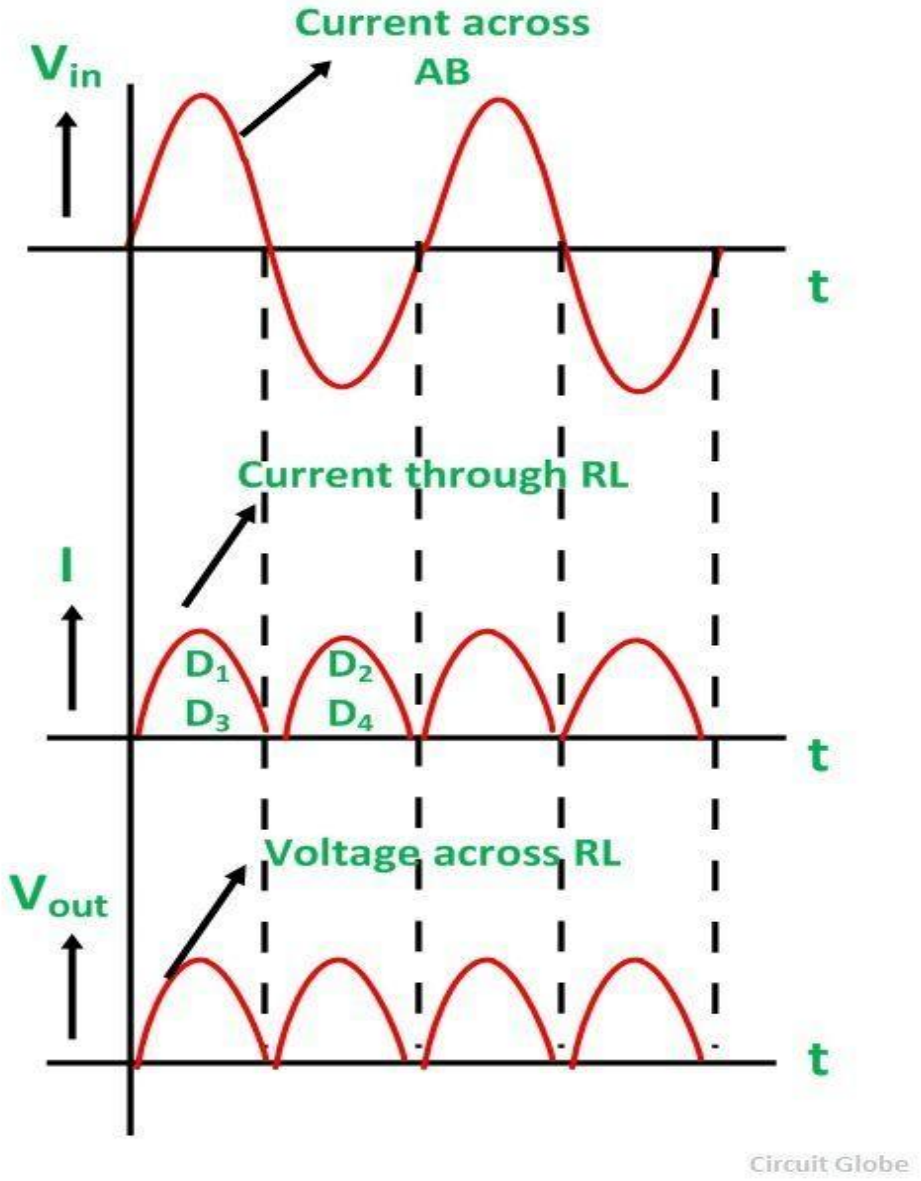
The diodes D_1 and D_3 are forward biased and the diodes D_2 and D_4 are reversed biased. Therefore, diode D_1 and D_3 conduct, and diode D_2 and D_4 do not conduct. The current (i) flows through diode D_1, load resistor R_L (from M to L), diode D_3, and the transformer secondary.



During the negative half-cycle, end A becomes negative and end B positive. the diode D_2 and D_4 are under forward bias and the diodes D_1 and D_3 are reverse bias. Therefore, diode D_2 and D_4 conduct while diodes D_1 and D_3 do not conduct. Thus, current (i) flows through the diode D_2, load resistor R_L (from M to L), diode D_4, and the transformer secondary.

The current flows through the load resistor R_L in the same direction (M to L) during both the half cycles. Hence, a DC output voltage V_{out} is obtained across the load resistor.





Wave form

Advantages:

- Step Down Transformer is not required.
- It has higher efficiency then half wave and full wave rectifier.
- The output waveform in continuous.
- To used in a device , a low level filter is required , so thus reducing the cost.

Disadvantages :

- Since four diodes are used , cost of making it increasing .
- The value of the diodes used should be precise , else there will be an error in rectification.
- The output is not a proper DC quantity. It has ripples in its output .

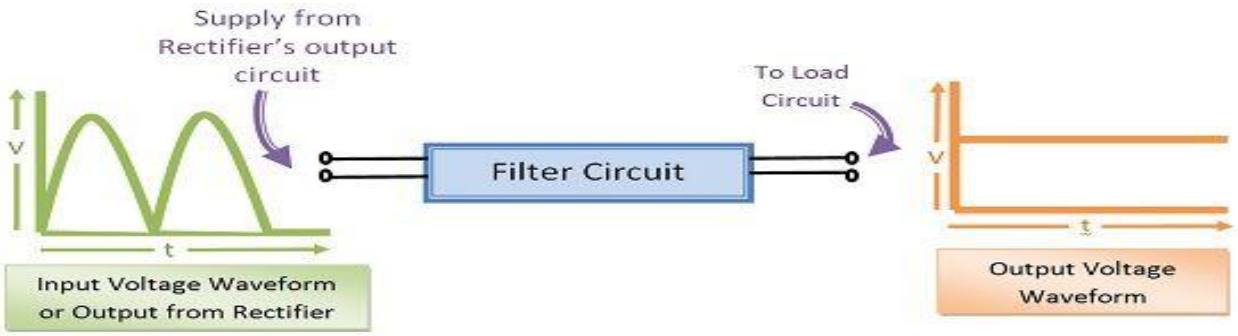
Filter circuit

Definition: **The** filter **circuit is necessary for smoothing of the voltage obtained by the rectifier. The obtained DC voltage contains AC components. These AC components are called** ripples. **The filter circuit is needed to remove the ripples from DC output voltage so that the output voltage across the load will be regulated.**

Filter Circuit is connected between the load and output of rectifier circuit. If this filter circuit is not connected between the rectifier and load the performance of the system will be poor because the output voltage will consist of AC ripples.

Components involved in filter Circuit

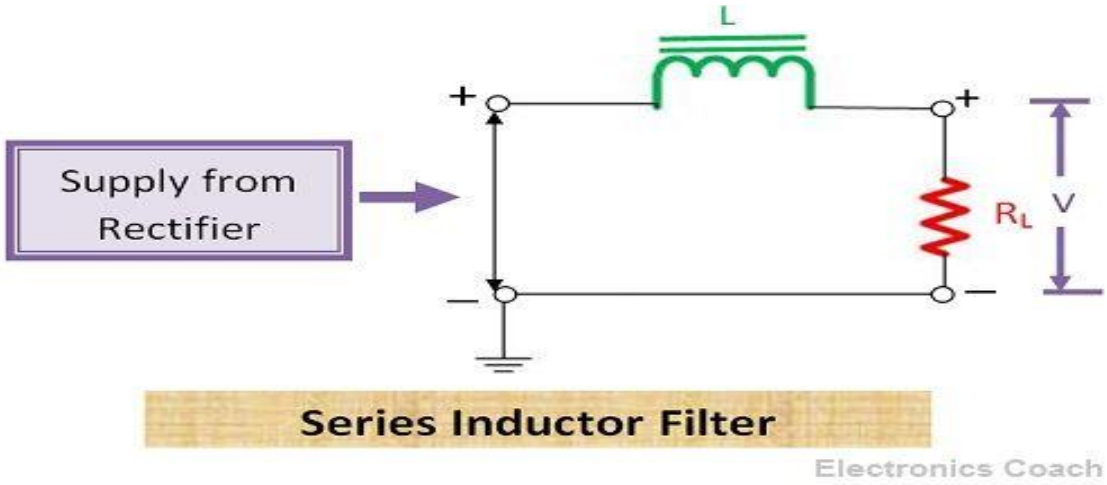
A filter circuit comprises of generally inductor and capacitor. The inductor allows DC only to pass through it and capacitor allows AC only to pass through it. Thus, a circuit formed by the combination of inductors and capacitors can effectively filters the signal according to the application.



Series Inductor Filter/choke input filter

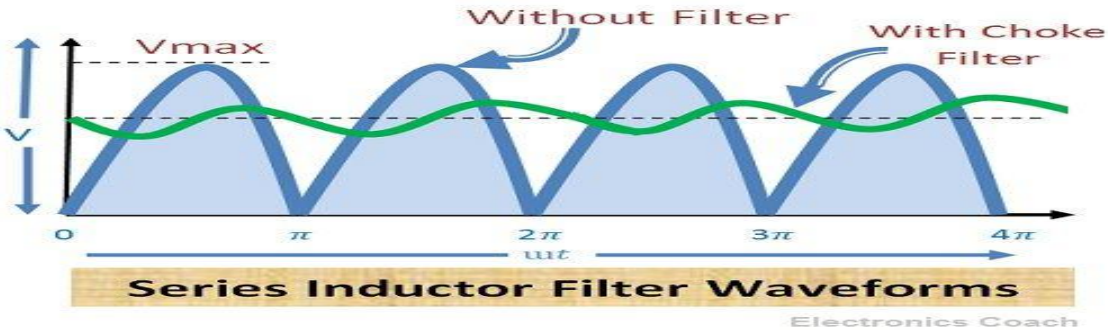
In series inductor filter the inductor is connected in series with the rectifier output and the load resistor. Thus, it is called series inductor filter. The property of an inductor to block AC and provides zero resistance to DC is used in filtering circuit. When the value of DC output from the rectifier is more than the average value then the rectifier store the excess current in the form of magnetic energy.

When the value of DC from the rectifier is less than the average value then the inductor release the stored magnetic energy in order to balance the effect of the low value of DC. In this way series inductor filter maintains the regulated DC supply. Moreover, inductor blocks the AC ripples present in the output voltage of rectifier; thus, smooth DC signal can be obtained.



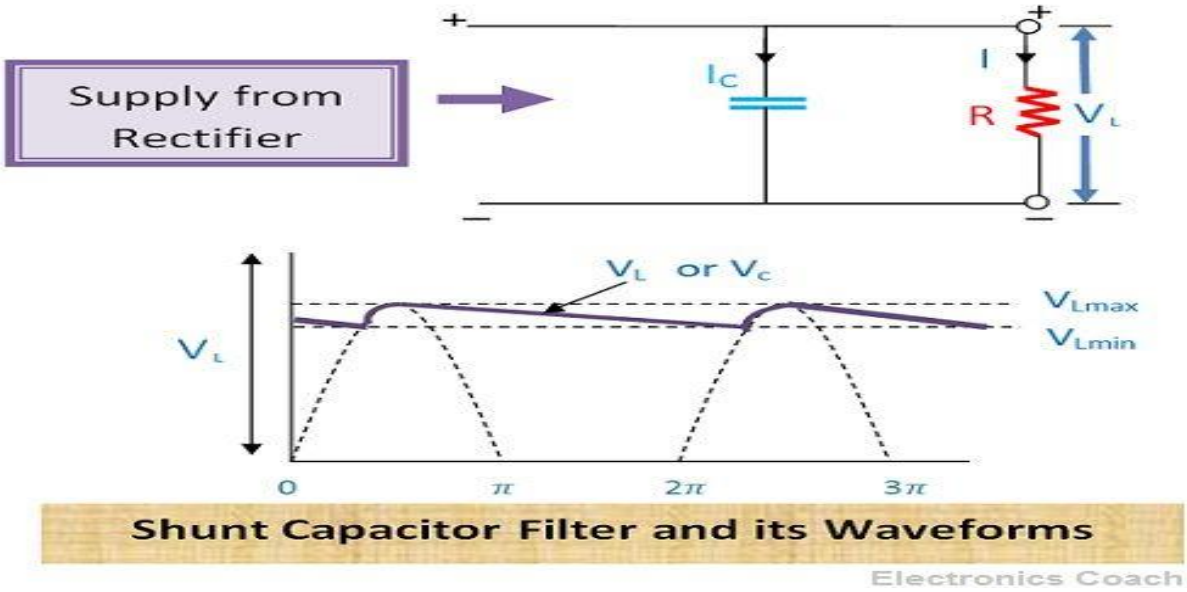
Waveforms of Series Inductor Filter

The waveform of series inductor filter is given in the below diagram. It can be seen that waveforms without filter consist of AC ripples while the waveform with filter is regulated.



Shunt Capacitor Filter

The Shunt capacitor filters comprise of capacitor along with the load resistor. In this, the capacitor is connected in parallel with respect to the output of rectifier circuit and also in parallel with the load resistor. During conduction, the capacitor starts charging and stores energy in the form of the electrostatic field. The capacitor will charge to its peak value because the charging time constant is almost zero.



During non-conduction, the capacitor will discharge through the load resistor. Thus, in this way, the capacitor will maintain constant output voltage and provide the regulated output. The shunt capacitor filters use the property of capacitor which blocks DC and provides low resistance to AC. Thus, AC ripples can bypass through the capacitor.

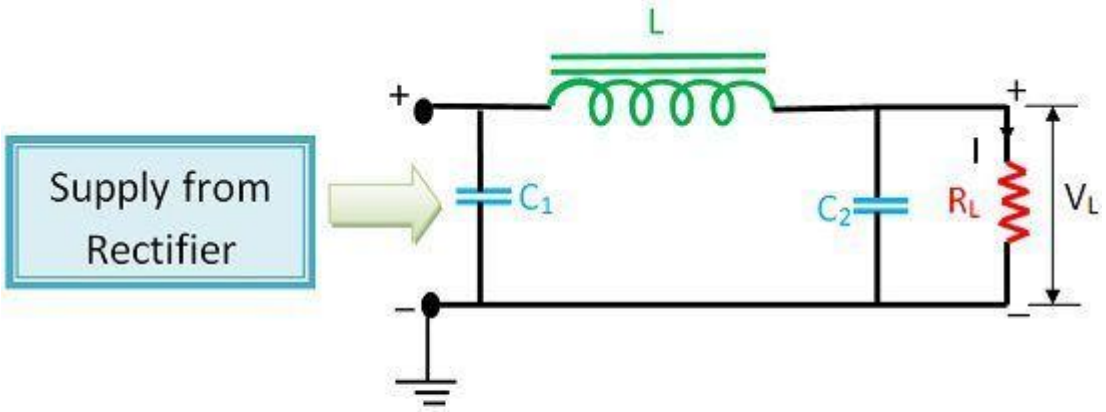
If the value of capacitance of the capacitor is high, then it will offer very low impedance to AC and extremely high impedance to DC. Thus, the AC ripples in the DC output voltage gets bypassed through parallel capacitor circuit, and DC voltage is obtained across the load resistor.

Pi filter (π- filter)

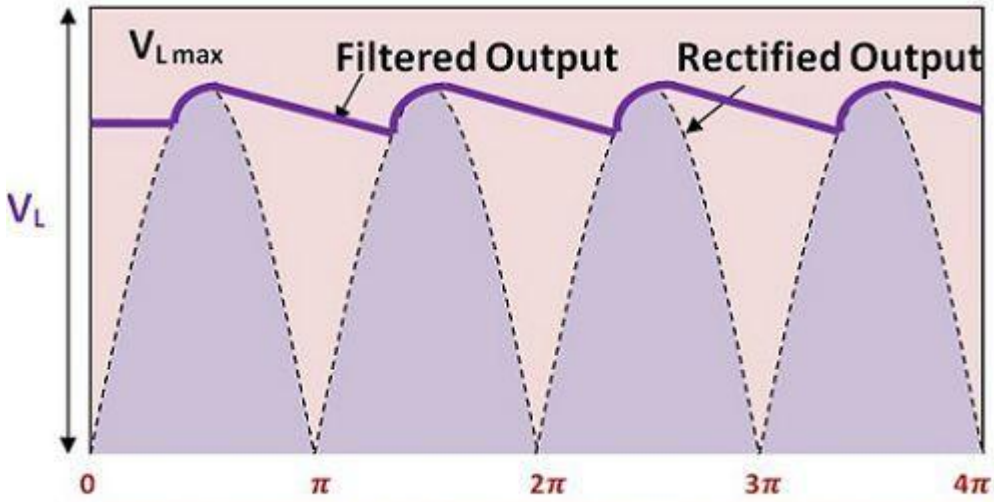
The output from the rectifier is directly applied to the input capacitor. The capacitor provides a low impedance to AC ripples present in the output voltage and high resistance to DC voltage. Therefore, most of the AC ripples get bypassed through the capacitor in input stage only.

The residual AC components which are still present in filtered DC signal gets filtered when they pass through the inductor coil and through the capacitor connected parallel across the load. In this way, the efficiency of filtering increases multiple times.

In the case of L-section filter, one inductor and capacitor were present so if some AC ripples say 1% is left after filtering that can be removed in Pi-filter. Thus, Pi filter is considered more efficient.



Capacitor Input Filter or Pi Filter



Output Voltage Waveform

CHAPTER-4

TRANSISTORS

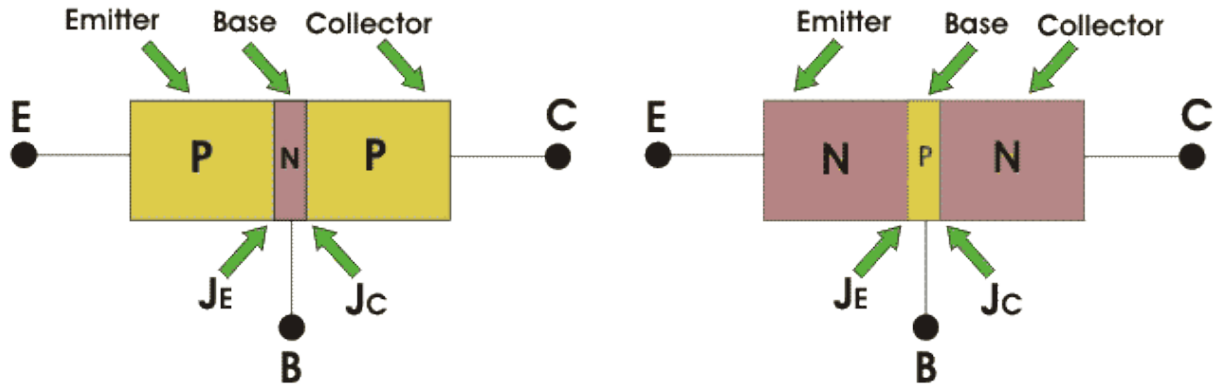
TRANSISTOR

A **transistor** is a semiconductor device used to amplify or switch electronic signals and electrical power. **Transistors** are one of the basic building blocks of modern electronics. It is composed of semiconductor material usually with at least three terminals for connection to an external circuit.

What is a BJT?

A Bipolar Junction Transistor (also known as a BJT or BJT Transistor) is a three-terminal semiconductor device consisting of two p-n junctions which are able to amplify or magnify a signal. It is a current controlled device. The three terminals of the BJT are the base, the collector and the emitter. A BJT is a type of transistor that uses both electrons and holes as charge carriers.

There are two types of bipolar junction transistors – NPN transistors and PNP transistors. A diagram of these two types of bipolar junction transistors is given below.

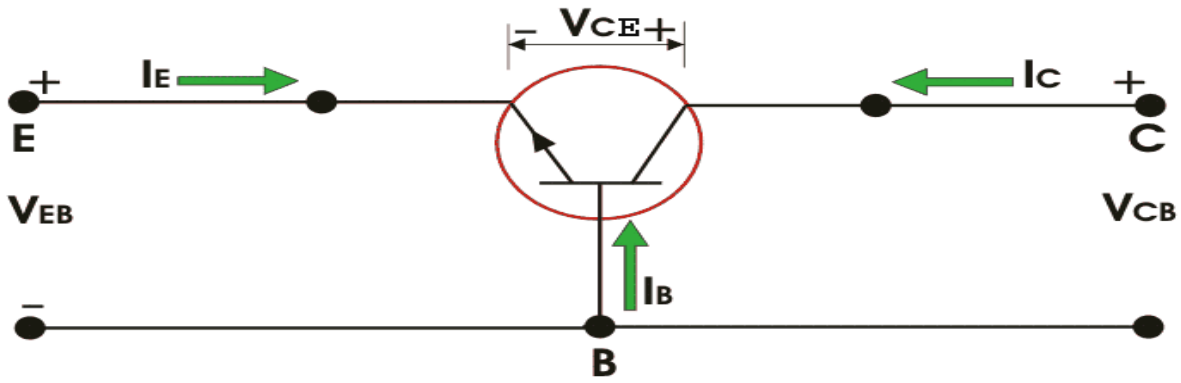


BJT has three parts named emitter, base and collector. J_E and J_C represent the junction of emitter and junction of collector respectively. The emitter based junction is forward biased and collector-base junctions are reverse biased.

DIFFERENT MODES OF OPERATION

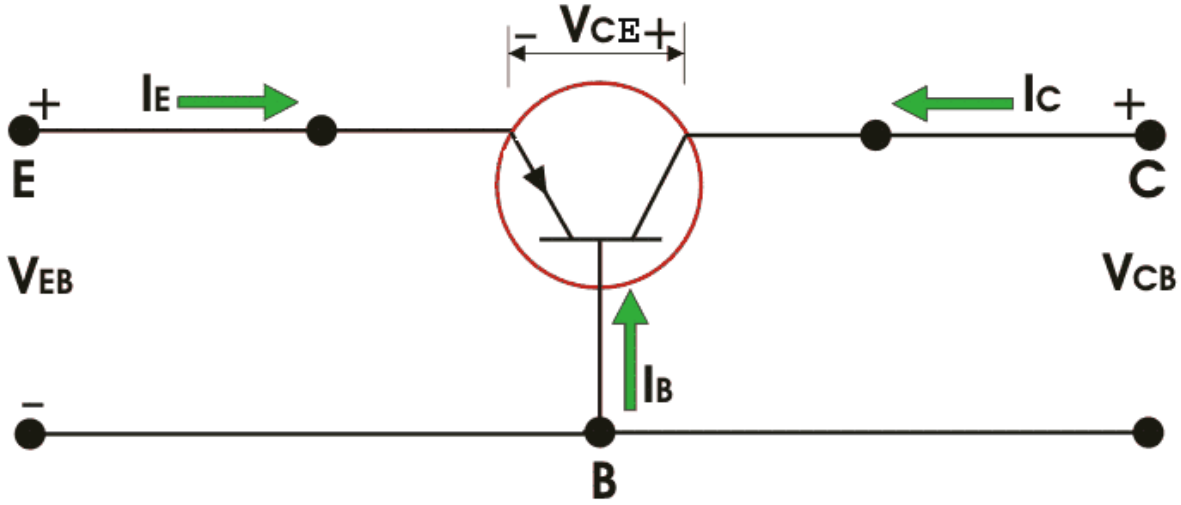
NPN Bipolar Junction Transistor

In an **n-p-n bipolar transistor** (or npn transistor) one p-type semiconductor resides between two n-type semiconductors the diagram below an n-p-n transistor is shown. I_E, I_C is emitter current and collect current respectively and V_{EB} and V_{CB} are emitter-base voltage and collector-base voltage respectively.



PNP Bipolar Junction Transistor

Similarly for **p-n-p bipolar junction** transistor (or pnp transistor), an n-type semiconductor is sandwiched between two p-type semiconductors. The diagram of a p-n-p transistor is shown below



For p-n-p transistors, current enters into the transistor through the emitter terminal. Like any bipolar junction transistor, the emitter-base junction is forward biased and the collector-base junction is reverse biased. We can tabulate the emitter, base and collector current, as well as the emitter-base, collector base and collector-emitter voltage for p-n-p transistors also.

Working Principle of BJT

- The figure shows an n-p-n transistor biased in the active region (See transistor biasing), the BE junction is forward biased whereas the CB junction is reversed biased. The width of the depletion region of the BE junction is small as compared to that of the CB junction.
- The forward bias at the BE junction reduces the barrier potential and causes the electrons to flow from the emitter to the base. As the base is thin and lightly doped it consists of very few holes so some of the electrons from the emitter (about 2%) recombine with the holes present in the base region and flow out of the base terminal.

- This constitutes the base current, it flows due to recombination of electrons and holes (Note that the direction of conventional current flow is opposite to that of the flow of electrons). The remaining large number of electrons will cross the reverse-biased collector junction to constitute the collector current. Thus by KCL,The base current is very small as compared to emitter and collector current.

  Here, the majority of charge carriers are electrons. The operation of a p-n-p transistor is same as of the n-p-n, the only difference is that the majority charge carriers are holes instead of electrons. Only a small part current flows due to majority carriers and most of the current flows due to minority charge carriers in a BJT. Hence, they are called as minority carrier devices.

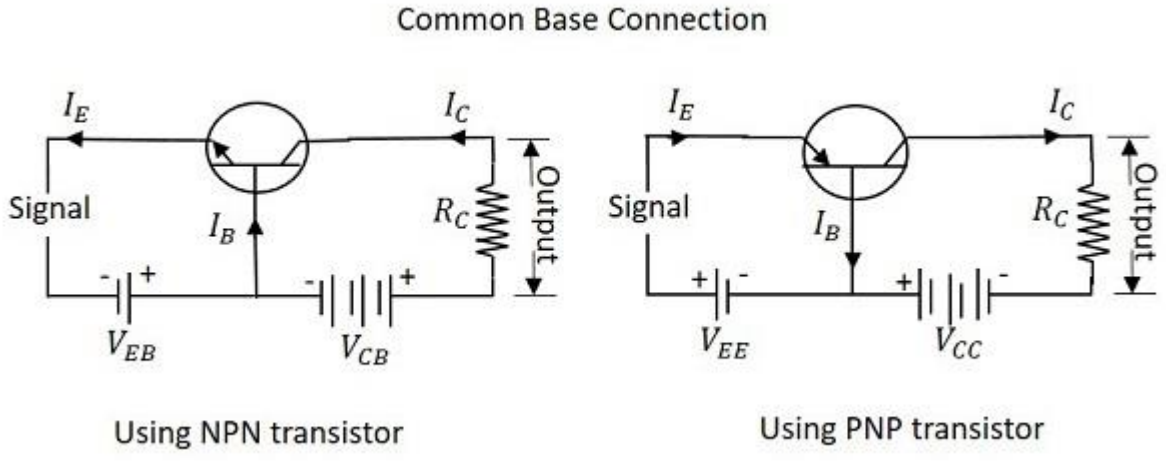
Transistor circuit configuration

A Transistor has 3 terminals, the emitter, the base and the collector. Using these 3 terminals the transistor can be connected in a circuit with one terminal common to both input and output in a 3 different possible configurations.

The three types of configurations are **Common Base, Common Emitter** and **Common Collector** configurations. In every configuration, the emitter junction is forward biased and the collector junction is reverse biased.

Common Base CB Configuration

The name itself implies that the Base terminal is taken as common terminal for both input and output of the transistor. The common base connection for both NPN and PNP transistors is as shown in the following figure.



let us consider NPN transistor in CB configuration. When the emitter voltage is applied, as it is forward biased, the electrons from the negative terminal repel the emitter electrons and current flows through the emitter and base to the collector to contribute collector current. The collector voltage $\mathbf{V_{CB}}$ is kept constant throughout this.

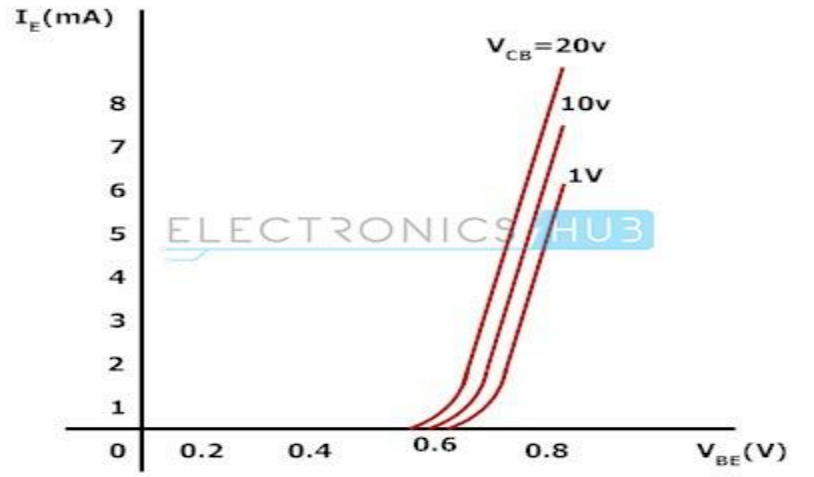
In the CB configuration, the input current is the emitter current $\mathbf{I_E}$ and the output current is the collector current $\mathbf{I_C}$.

Current Amplification Factor α

The ratio of change in collector current ΔI_C to the change in emitter current ΔI_E when collector voltage $\mathbf{V_{CB}}$ is kept constant, is called as **Current amplification factor**. It is denoted by α.

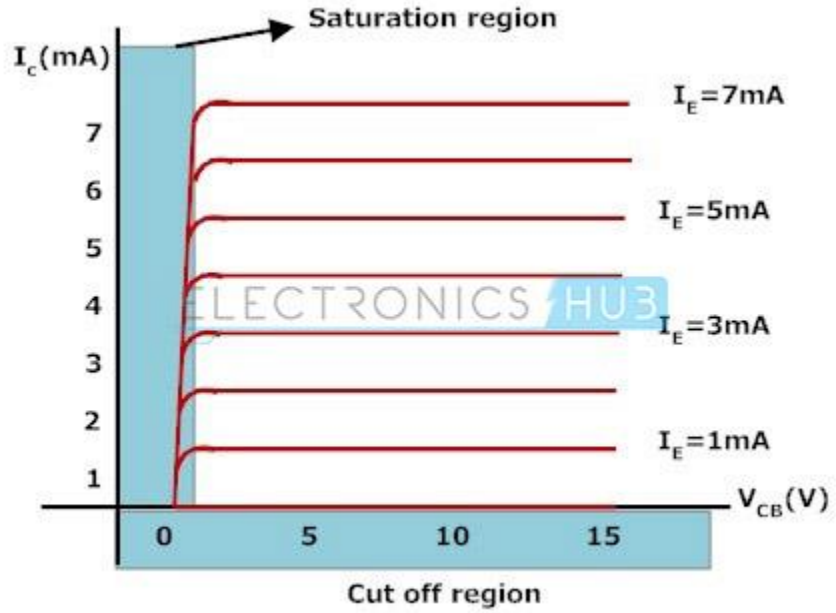
$$\alpha = \Delta I_C / \Delta I_E \text{ at constant } V_{CB}$$

Input Characteristics



$R_{in} = V_{EB} / I_E$ (when V_{CB} is constant)

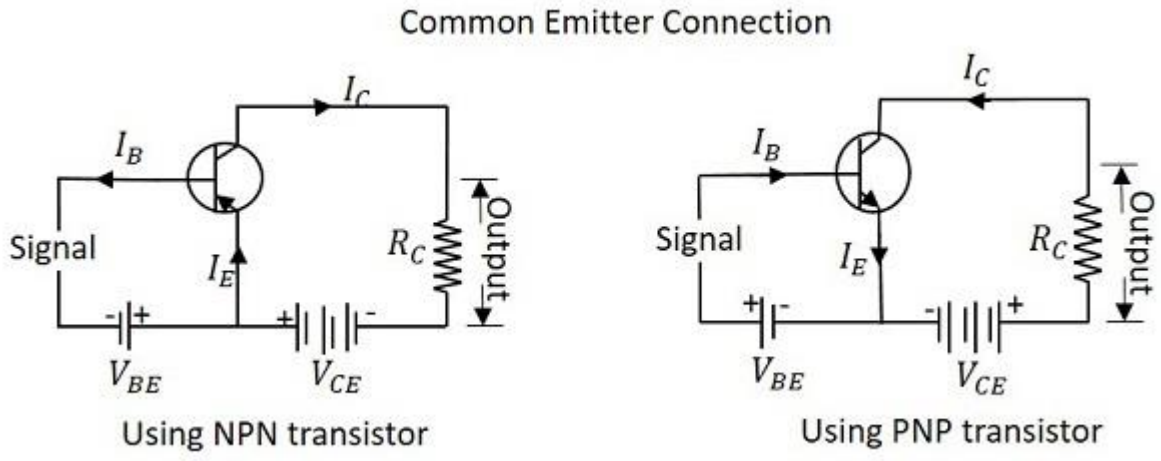
Output Characteristics



$R_{out} = V_{CB} / I_C$ (when I_E is constant)

Common Emitter CE Configuration

The name itself implies that the **Emitter** terminal is taken as common terminal for both input and output of the transistor. The common emitter connection for both NPN and PNP transistors is as shown in the following figure.



As in CB configuration, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is the base current $\mathbf{I_B}$ and the output current is the collector current $\mathbf{I_C}$ here.

Base Current Amplification factor β

The ratio of change in collector current ΔI_C to the change in base current ΔI_B is known as **Base Current Amplification Factor**. It is denoted by β

$$\beta=\Delta I_C/\Delta I_B$$

Relation between β and α

Let us try to derive the relation between base current amplification factor and emitter current amplification factor.

$$\beta=\Delta I_C/\Delta I_B$$

$$\alpha=\Delta I_C/\Delta I_E$$

$$I_E=I_B+I_C$$

$$\Delta I_E=\Delta I_B+\Delta I_C$$

$$\Delta I_B=\Delta I_E-\Delta I_C$$

We can write

$$\beta=\Delta I_C/\Delta I_E-\Delta I_C$$

Dividing by ΔI_E

$$\beta = \frac{\Delta IC/\Delta IE}{\Delta IE/\Delta IE - \Delta IC/\Delta IE}$$

Put the value of $\alpha = \Delta I_C/\Delta I_E$ In the above equation

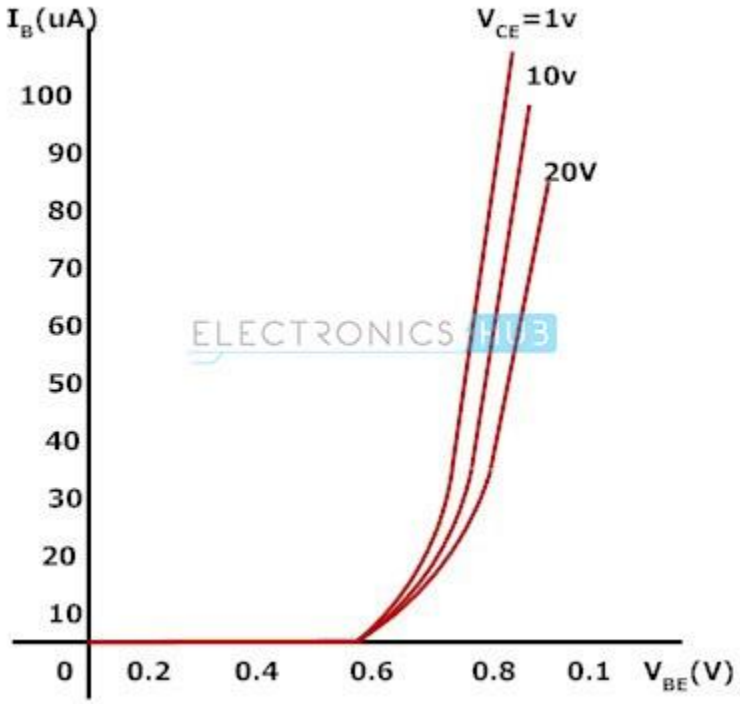
We get $\beta = \frac{\alpha}{1-\alpha}$

From the above equation, it is evident that, as α approaches 1, β reaches infinity.

Hence, **the current gain in Common Emitter connection is very high**. This is the reason this circuit connection is mostly used in all transistor applications.

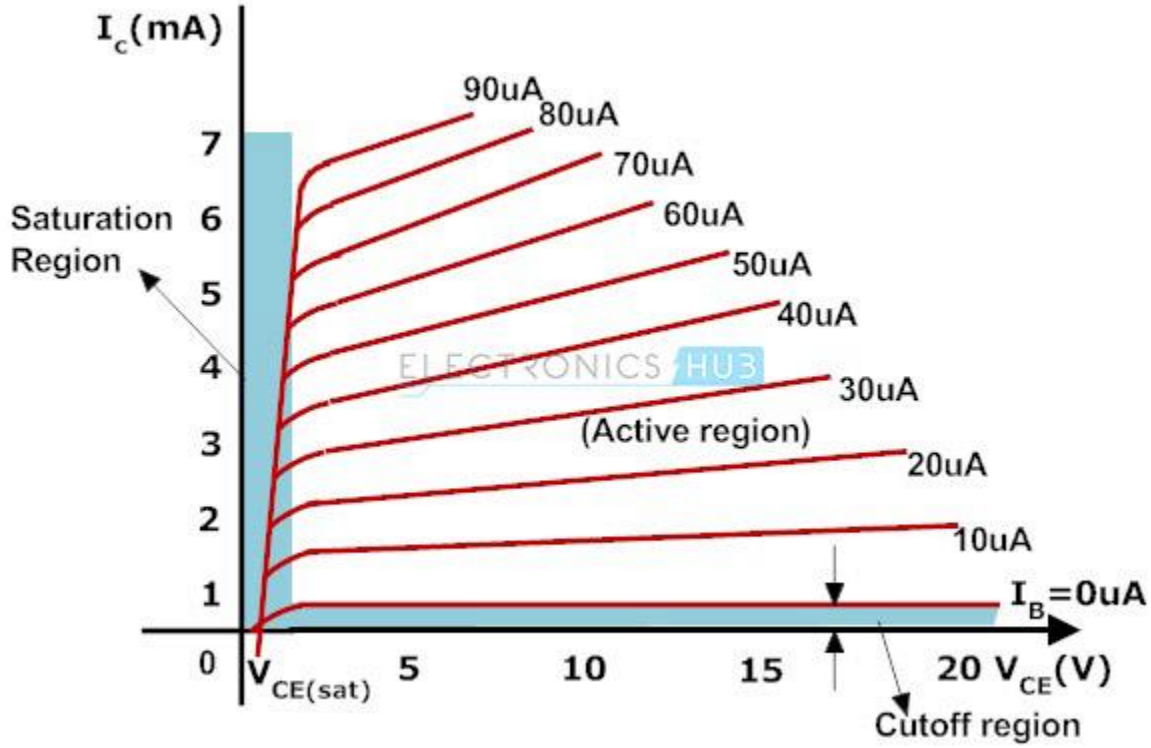
Input Characteristics

$R_{in} = V_{BE}/I_B$ (when V_{CE} is at constant)



output Characteristics

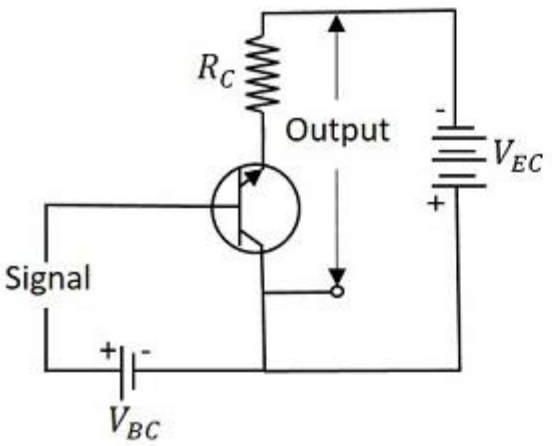
$R_{out} = V_{CE}/I_C$ (when I_B is at constant)



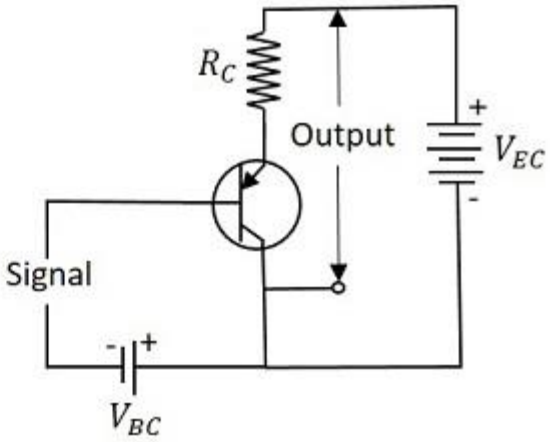
Common Collector CC Configuration

The name itself implies that the **Collector** terminal is taken as common terminal for both input and output of the transistor. The common collector connection for both NPN and PNP transistors is as shown in the following figure.

Common Collector Connection



Using NPN transistor



Using PNP transistor

Just as in CB and CE configurations, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is the base current I_B and the output current is the emitter current I_E here.

Current Amplification Factor γ

The ratio of change in emitter current ΔI_E to the change in base current ΔI_B is known as **Current Amplification factor** in common collector CC configuration. It is denoted by **γ**.

$$\gamma = \Delta I_E / \Delta I_B$$

- The current gain in CC configuration is same as in CE configuration.
- The voltage gain in CC configuration is always less than 1.

Relation between γ and α

$$\gamma = \Delta I_E / \Delta I_B$$

$$\alpha = \Delta I_C / \Delta I_E$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of I_B, we get

$$\gamma = \Delta I_E / \Delta I_E - \Delta I_C$$

Dividing by ΔI_E

$$\gamma = \frac{\Delta IE/\Delta IE}{\Delta IE/\Delta IE - \Delta IC/\Delta IE}$$

$$\gamma = \frac{\mathbf{1}}{\mathbf{1-\alpha}}$$

- The voltage gain provided by this circuit is less than 1.

CHAPTER-5

TRANSISTOR CIRCUITS

Transistor circuit

Transistor Biasing

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

For a transistor to be operated as a faithful amplifier, the operating point should be stabilized

Factors affecting the operating point

The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.

As temperature increases, the values of I_{CE}, β, V_{BE} gets affected.

Stabilization

The process of making the operating point independent of temperature changes or variations in transistor parameters is known as **Stabilization**.

Need for Stabilization

Stabilization of the operating point has to be achieved due to the following reasons.

- Temperature dependence of I_c
- Individual variations
- Thermal runaway

Temperature Dependence of I_C

As the expression for collector current I_c is

$$I_C=\beta I_B+I_{CEO}$$

$$=\beta I_B+(\beta+1)I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced by temperature variations. To come out of this, the biasing conditions are set so that zero signal collector current I_c = 1 mA. Therefore, the operating point needs to be stabilized i.e. it is necessary to keep I_c constant.

Individual Variations

As the value of β and the value of V_{BE} are not same for every transistor, whenever a transistor is replaced, the operating point tends to change. Hence it is necessary to stabilize the operating point.

Thermal Runaway

The self-destruction of such an unstabilized transistor is known as **Thermal run away**.

In order to avoid **thermal runaway** and the destruction of transistor, it is necessary to stabilize the operating point, i.e., to keep I_c constant.

Stability Factor

the rate of change of collector current I_c with respect to the collector leakage current I_{co} at constant β and I_B is called **Stability factor**.

$$S=dI_C/dI_{CO} \quad \text{at constant } I_B \text{ and } \beta$$

Hence we can understand that any change in collector leakage current changes the collector current to a great extent. The stability factor should be as low as possible so that the collector current doesn't get affected. S=1 is the ideal value**.**

Different method of transistor biasing

The commonly used methods of transistor biasing are

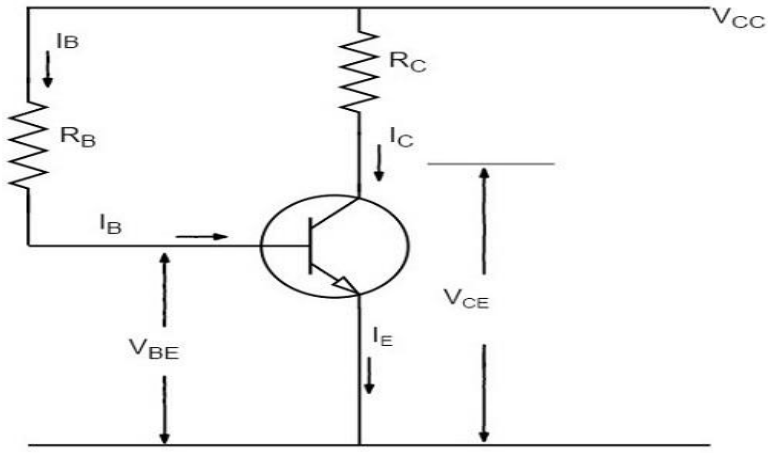
- Base Resistor method
- Collector to Base bias
- Voltage-divider bias

All of these methods have the same basic principle of obtaining the required value of I_B and I_c from V_{cc} in the zero signal conditions.

Base Resistor Method

In this method, a resistor R_B of high resistance is connected in base, as the name implies. The required zero signal base current is provided by V_{cc} which flows through R_B. The base emitter junction is forward biased, as base is positive with respect to emitter.

The required value of zero signal base current and hence the collector current (as $I_c = \beta I_B$) can be made to flow by selecting the proper value of base resistor RB. Hence the value of R_B is to be known. The figure below shows how a base resistor method of biasing circuit looks like.



Let I_c be the required zero signal collector current. Therefore,

$$I_B=I_C/\beta$$

Considering the closed circuit from V_{cc}, base, emitter and ground, while applying the Kirchhoff's voltage law, we get,

$$V_{CC}=I_BR_B+V_{BE}$$

$$I_BR_B=V_{CC}-V_{BE}$$

Therefore

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

Since V_{BE} is generally quite small as compared to V_{cc}, the former can be neglected with little error. Then,

$$R_B = \frac{V_{CC}}{I_B}$$

We know that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. As R_B can be found directly, this method is called as **fixed bias method**.

Stability factor, $S = \beta + 1$

Thus the stability factor in a fixed bias is (β+1) which means that I_c changes (β+1) times as much as any change in I_{co}.

Advantages

- The circuit is simple.
- Only one resistor R_E is required.
- Biasing conditions are set easily.
- No loading effect as no resistor is present at base-emitter junction.

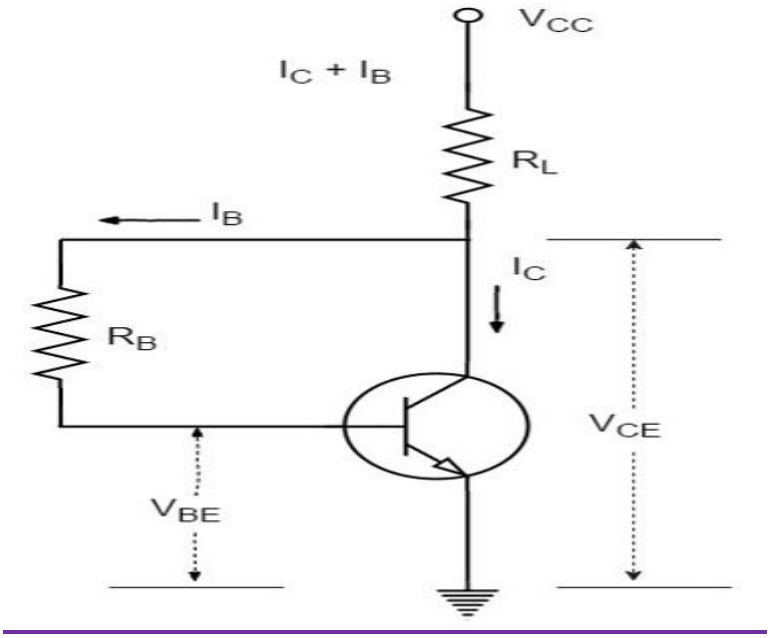
Disadvantages

- The stabilization is poor as heat development can't be stopped.
- The stability factor is very high. So, there are strong chances of thermal run away.

Hence, this method is rarely employed.

Collector to Base Bias

The collector to base bias circuit is same as base bias circuit except that the base resistor R_B is returned to collector, rather than to V_{CC} supply as shown in the figure below.



This circuit helps in improving the stability considerably. If the value of I_C increases, the voltage across R_L increases and hence the V_{CE} also increases. This in turn reduces the base current I_B. This action somewhat compensates the original increase.

The required value of R_B needed to give the zero signal collector current I_C can be calculated as follows.

Voltage drop across R_L will be

$$R_L=(I_C+I_B)R_L \cong I_C R_L$$

From the figure,

$$I_C R_L+I_B R_B+V_{BE}=V_{CC}$$

Or

$$I_B R_B= V_{CC}-V_{BE}-I_C R_L$$

Therefore

$$R_B= \frac{V_{CC}-V_{BE}-I_C R_L}{I_B}$$

$$R_B= \frac{(V_{CC}-V_{BE}-I_C R_L)\beta}{I_C}$$

Applying KVL we have

$$(I_B+I_C)R_L+I_B R_B+V_{BE}=V_{CC}$$

Or

$$I_B(R_L+R_B)+I_C R_L+V_{BE}=V_{CC}$$

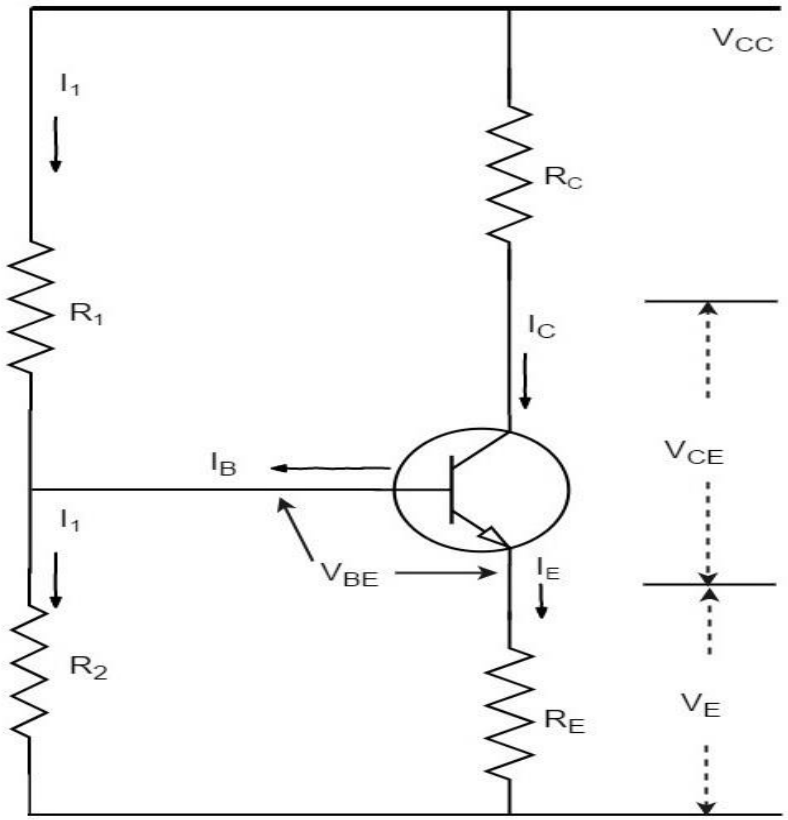
Therefore

$$I_B= \frac{V_{CC}-V_{BE}-I_C R_L}{R_L+R_B}$$

Voltage Divider Bias Method

Among all the methods of providing biasing and stabilization, the **voltage divider bias method** is the most prominent one. Here, two resistors R_1 and R_2 are employed, which are connected to V_{cc} and provide biasing. The resistor R_E employed in the emitter provides stabilization.

The name voltage divider comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero signal conditions. The figure below shows the circuit of voltage divider bias method.



Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

Now let us try to derive the expressions for collector current and collector voltage.

Collector Current, I_C

From the circuit, it is evident that,

$$I_1 = \frac{V_{CC}}{R_1+R_2}$$

Therefore, the voltage across resistance R_2 is

$$V_2 = (V_{CC} / R_1+R_2)\, R_2$$

Applying Kirchhoff's voltage law to the base circuit,

$$V_2 = V_{BE}+V_E$$

$$V_2 = V_{BE}+I_E R_E$$

$$I_E = \frac{V_2-V_{BE}}{R_E}$$

Since $I_E \approx I_C$,

$$I_C = \frac{V_2-V_{BE}}{R_E}$$

From the above expression, it is evident that I_C doesn't depend upon β. V_{BE} is very small that I_C doesn't get affected by V_{BE} at all. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilization is achieved.

Collector-Emitter Voltage, V_{CE}

Applying Kirchhoff's voltage law to the collector side,

$$V_{CC}=I_CR_C+V_{CE}+I_ER_E$$

Since $I_E \cong I_C$

$$=I_CR_C+V_{CE}+I_CR_E$$

$$=I_C(R_C+R_E)+V_{CE}$$

Therefore,

$$V_{CE}=V_{CC}-I_C(R_C+R_E)$$

R_E provides excellent stabilization in this circuit.

$$V_2=V_{BE}+I_CR_E$$

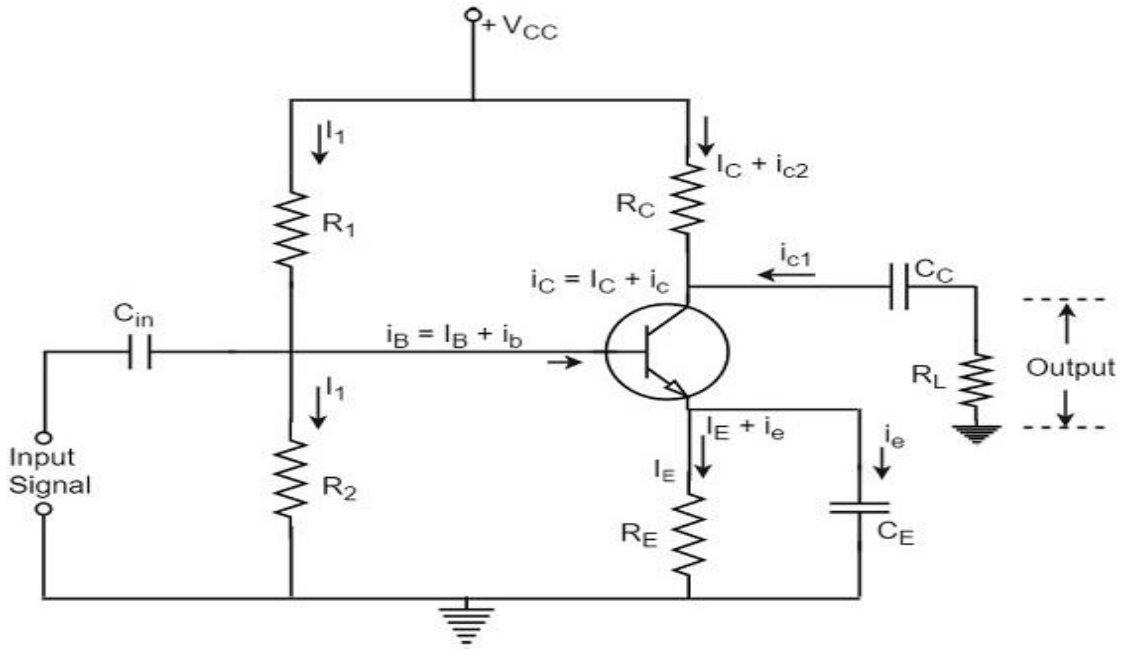
Stability Factor =

$$S=(\beta+1)\times \frac{1}{(\beta+1)}=1$$

TRANSISTOR AMPLIFIER AND OSCILLATORS

Practical Circuit of a Transistor Amplifier

The circuit of a practical transistor amplifier is as shown below, which represents a voltage divider biasing circuit.



The various circuit elements and their functions are as described below.

Biasing Circuit

The resistors R_1, R_2 and R_E form the biasing and stabilization circuit, which helps in establishing a proper operating point.

Input Capacitor C_{in}

This capacitor couples the input signal to the base of the transistor. The input capacitor C_{in} allows AC signal, but isolates the signal source from R_2. If this capacitor is not present, the input signal gets directly applied, which changes the bias at R_2.

Coupling Capacitor C_C

This capacitor is present at the end of one stage and connects it to the other stage. As it couples two stages it is called as **coupling capacitor**. This capacitor blocks DC of one stage to enter the other but allows AC to pass. Hence it is also called as **blocking capacitor**.

Due to the presence of coupling capacitor C_C, the output across the resistor R_L is free from the collector's DC voltage. If this is not present, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C, as it would come in parallel to R_2 of the next stage.

Emitter by-pass capacitor C_E

This capacitor is employed in parallel to the emitter resistor R_E. The amplified AC signal is by passed through this. If this is not present, that signal will pass through R_E which produces a voltage drop across R_E that will feedback the input signal reducing the output voltage.

The Load resistor R_L

The resistance R_L connected at the output is known as **Load resistor**. When a number of stages are used, then R_L represents the input resistance of the next stage.

Various Circuit currents

Let us go through various circuit currents in the complete amplifier circuit. These are already mentioned in the above figure.

Base Current

When no signal is applied in the base circuit, DC base current I_B flows due to biasing circuit. When AC signal is applied, AC base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by

$$i_B = I_B + i_b$$

Collector Current

When no signal is applied, a DC collector current I_C flows due to biasing circuit. When AC signal is applied, AC collector current i_c also flows. Therefore, the total collector current i_C is given by

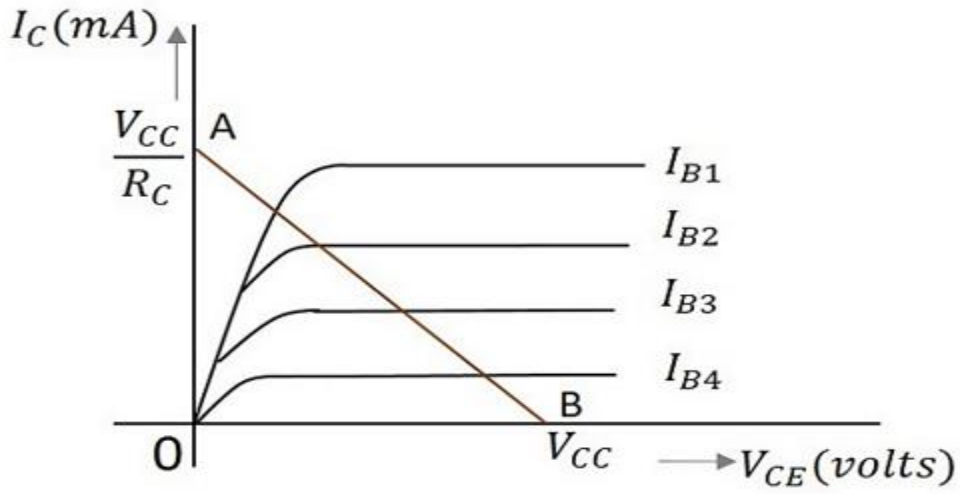
$$i_C = I_C + i_c$$

Emitter Current

When no signal is applied, a DC emitter current I_E flows. With the application of signal, total emitter current i_E is given by

$$i_E = I_E + i_e$$

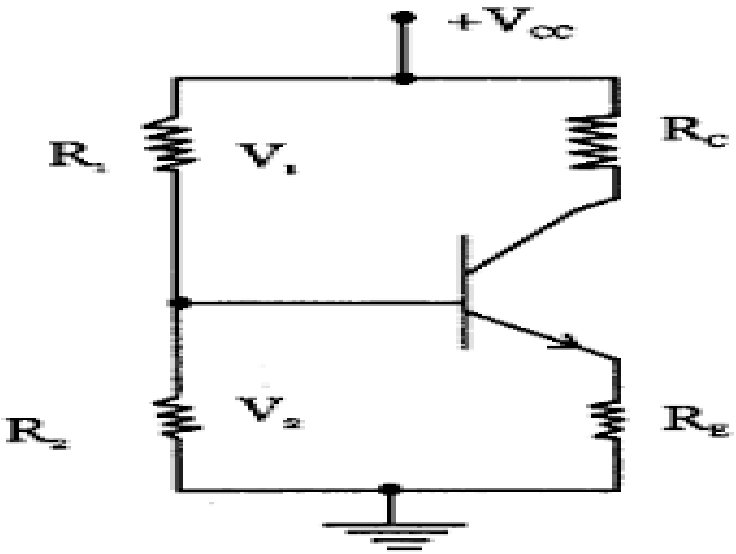
DC LOAD LINE



In graphical analysis of nonlinear electronic circuits, a **load line** is a line drawn on the characteristic curve, a graph of the current vs. the voltage in a nonlinear device like a diode or transistor.

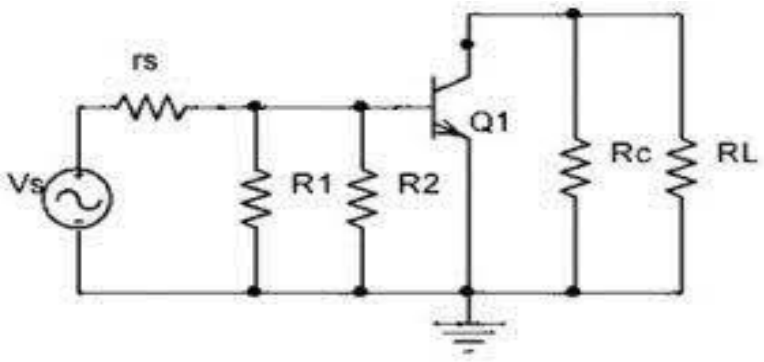
DC EQUIVALENT CKT

A **DC equivalent** of a **circuit** can be constructed by replacing all capacitances with open **circuits**, inductances with short **circuits**, and reducing AC sources to zero (replacing AC voltage sources by short **circuits** and AC current sources by open **circuits**.)



AC EQUIVALENT CKT

An **AC equivalent circuit** can be constructed by reducing all DC sources to zero (replacing DC voltage sources with short **circuits** and DC current sources with open **circuits**)



MULTISTAGE TRANSISTOR AMPLIFIERS.

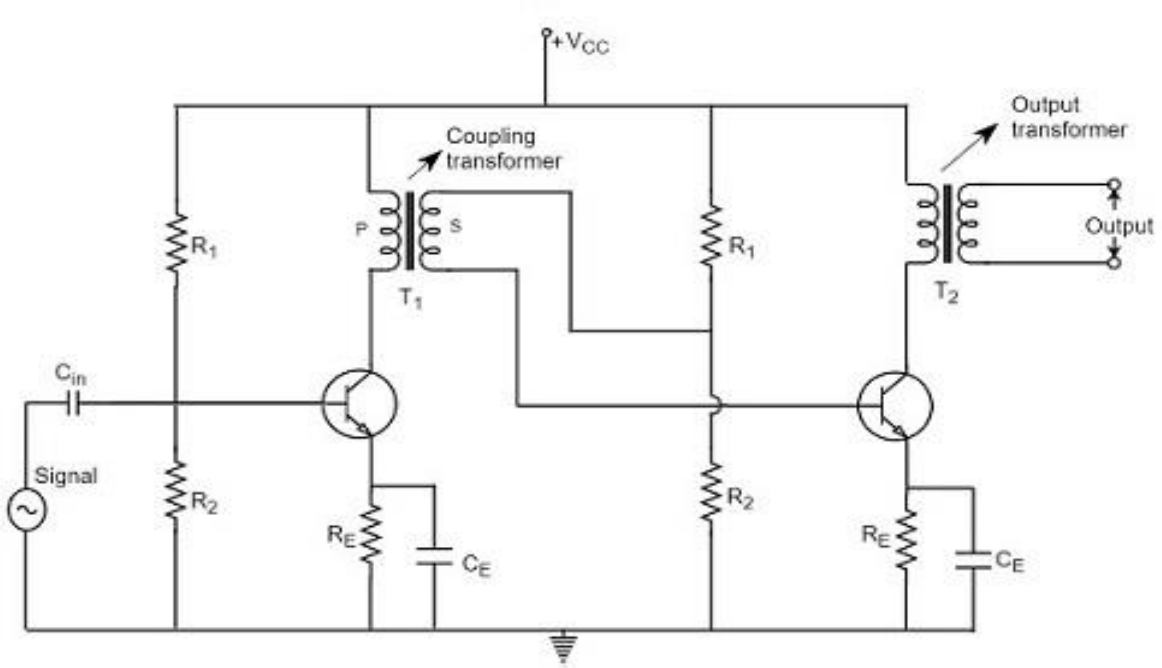
Definition: An **amplifier** formed by connecting several **amplifiers** in cascaded arrangement such that output of one **amplifier** becomes the input of other whose output becomes input of next and so on . Each **amplifier** in this configuration is known as stage.

Transformer Coupled Amplifier

The amplifier circuit in which, the previous stage is connected to the next stage using a coupling transformer, is called as Transformer coupled amplifier.

The coupling transformer T_1 is used to feed the output of 1st stage to the input of 2nd stage. The collector load is replaced by the primary winding of the transformer. The secondary winding is connected between the potential divider and the base of 2nd stage, which provides the input to the 2nd stage. Instead of coupling capacitor like in RC coupled amplifier, a transformer is used for coupling any two stages, in the transformer coupled amplifier circuit.

The figure below shows the circuit diagram of transformer coupled amplifier.



Operation of Transformer Coupled Amplifier

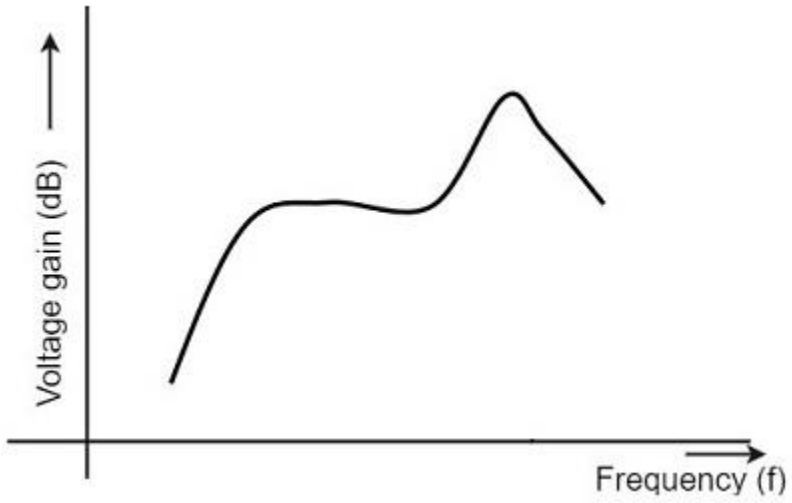
When an AC signal is applied to the input of the base of the first transistor then it gets amplified by the transistor and appears at the collector to which the primary of the transformer is connected.

The transformer which is used as a coupling device in this circuit has the property of impedance changing, which means the low resistance of a stage (or load) can be reflected as a high load resistance to the previous stage. Hence the voltage at the primary is transferred according to the turns ratio of the secondary winding of the transformer.

This transformer coupling provides good impedance matching between the stages of amplifier. The transformer coupled amplifier is generally used for power amplification.

Frequency Response of Transformer Coupled Amplifier

The figure below shows the frequency response of a transformer coupled amplifier. The gain of the amplifier is constant only for a small range of frequencies. The output voltage is equal to the collector current multiplied by the reactance of primary.



Advantages of Transformer Coupled Amplifier

The following are the advantages of a transformer coupled amplifier −

- An excellent impedance matching is provided.
- Gain achieved is higher.
- There will be no power loss in collector and base resistors.
- Efficient in operation.

Disadvantages of Transformer Coupled Amplifier

The following are the disadvantages of a transformer coupled amplifier −

- Though the gain is high, it varies considerably with frequency. Hence a poor frequency response.
- Frequency distortion is higher.
- Transformers tend to produce hum noise.
- Transformers are bulky and costly.

Applications

The following are the applications of a transformer coupled amplifier −

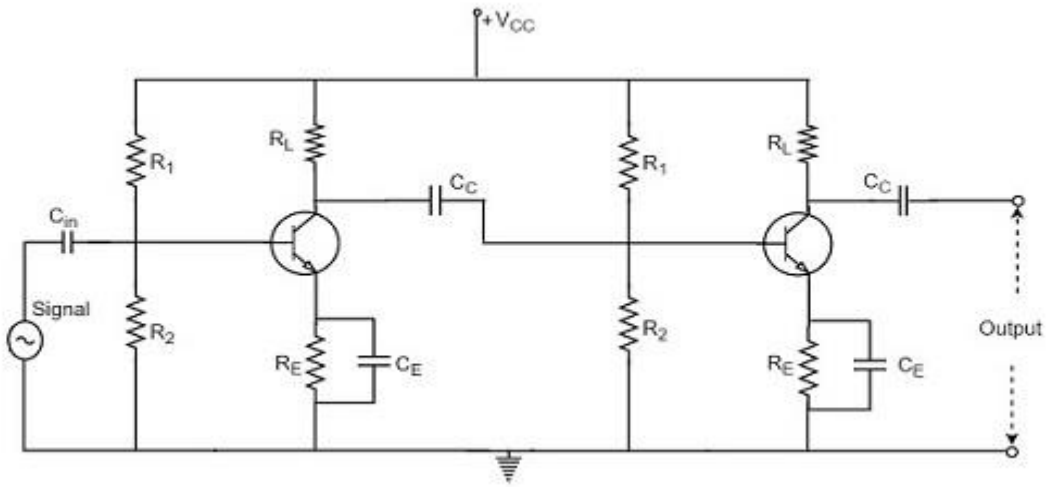
- Mostly used for impedance matching purposes.
- Used for Power amplification.
- Used in applications where maximum power transfer is needed.

Two-stage RC Coupled Amplifier

The constructional details of a two-stage RC coupled transistor amplifier circuit are as follows. The two stage amplifier circuit has two transistors, connected in CE configuration and a common power supply V_{cc} is used. The potential divider

network R_1 and R_2 and the resistor R_e form the biasing and stabilization network. The emitter by-pass capacitor C_e offers a low reactance path to the signal.

The resistor R_L is used as a load impedance. The input capacitor C_{in} present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point. The figure below shows the circuit diagram of RC coupled amplifier.



Operation of RC Coupled Amplifier

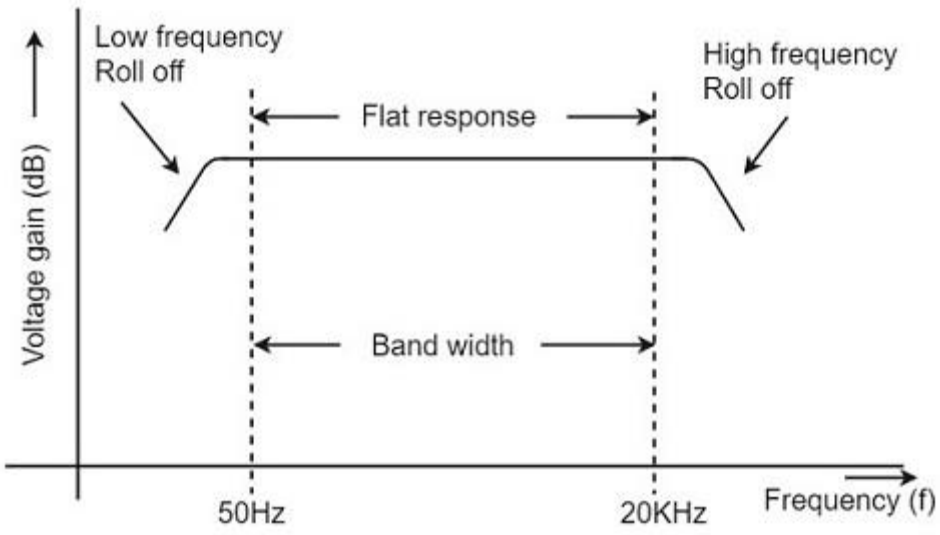
When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load R_L which is then passed through the coupling capacitor C_C to the next stage. This becomes the input of the next stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages. This is because when a second stage is made to follow the first stage, the **effective load resistance** of the first stage is reduced due to the shunting effect of the input resistance of the second stage. Hence, in a multistage amplifier, only the gain of the last stage remains unchanged.

As we consider a two stage amplifier here, the output phase is same as input. Because the phase reversal is done two times by the two stage CE configured amplifier circuit.

Frequency Response of RC Coupled Amplifier

Frequency response curve is a graph that indicates the relationship between voltage gain and function of frequency. The frequency response of a RC coupled amplifier is as shown in the following graph.



At Low frequencies (i.e. below 50 Hz)

The capacitive reactance is inversely proportional to the frequency. At low frequencies, the reactance is quite high. The reactance of input capacitor C_{in} and the coupling capacitor C_c are so high that only small part of the input signal is allowed. The reactance of the emitter by pass capacitor C_E is also very high during low frequencies. Hence it cannot shunt the emitter resistance effectively. With all these factors, the voltage gain rolls off at low frequencies.

At High frequencies (i.e. above 20 KHz)

Again considering the same point, we know that the capacitive reactance is low at high frequencies. So, a capacitor behaves as a short circuit, at high frequencies. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Along with this, as the capacitance of emitter diode decreases, it increases the base current of the transistor due to which the current gain (β) reduces. Hence the voltage gain rolls off at high frequencies.

At Mid-frequencies (i.e. 50 Hz to 20 KHz)

The voltage gain of the capacitors is maintained constant in this range of frequencies, as shown in figure. If the frequency increases, the reactance of the capacitor C_c decreases which tends to increase the gain. But this lower capacitance reactive increases the loading effect of the next stage by which there is a reduction in gain.

Due to these two factors, the gain is maintained constant.

Advantages of RC Coupled Amplifier

The following are the advantages of RC coupled amplifier.

- The frequency response of RC amplifier provides constant gain over a wide frequency range, hence most suitable for audio applications.
- The circuit is simple and has lower cost because it employs resistors and capacitors which are cheap.
- It becomes more compact with the upgrading technology.

Disadvantages of RC Coupled Amplifier

The following are the disadvantages of RC coupled amplifier.

- The voltage and power gain are low because of the effective load resistance.
- They become noisy with age.

- Due to poor impedance matching, power transfer will be low.

Applications of RC Coupled Amplifier

The following are the applications of RC coupled amplifier.

- They have excellent audio fidelity over a wide range of frequency.
- Widely used as Voltage amplifiers
- Due to poor impedance matching, RC coupling is rarely used in the final stages.

Difference Between Voltage And Power Amplifier

Voltage Amplifier

1. The voltage amplifier amplifies the voltage or increases the voltage level of a signal.
2. The voltage amplifier can work with low magnitude signal.
3. The transistor used in the voltage amplifier has a thin base because it does not handle large current.
4. The transistor used can dissipate less heat produced during its operation.
5. The physical size of transistor used is usually small and is known as low or medium power transistor.
6. RC coupling is used in voltage amplifier.
7. In power amplifier, the collector load has low resistance, typically 5Ω to 20Ω.
8. Voltage amplifier is used for small signal voltage.
9. The current gain of the voltage amplifier is very low.

Power Amplifier

1. The power amplifier amplifies the power of a signal.
2. The input signal of the power amplifier must have a high magnitude.
3. The transistor used in the power amplifier has a thick base because it handles the very large current.
4. The transistor used can dissipate more heat produced as compared to voltage amplifier during its operation.
5. The physical size of transistor used is usually large and is known as power transistor.
6. Transformer coupling is used in power amplifier.
7. In voltage amplifier, the collector load has high resistance, typically 4Ω to 10kΩ.
8. Power amplifier is used for high voltage signals.
9. The current gain of the power amplifier is very high.

power amplifier classification

The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor, plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.

On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.

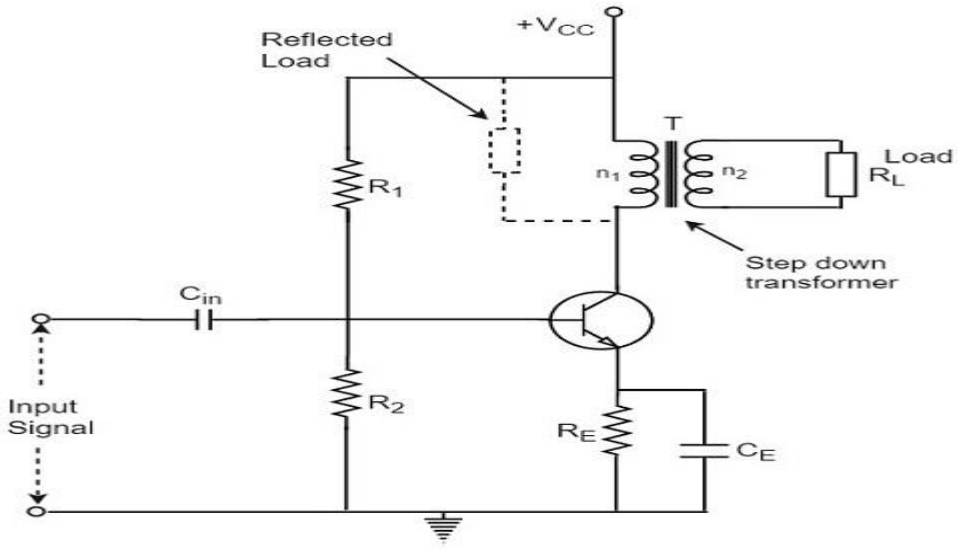
- **Class A Power amplifier** − When the collector current flows at all times during the full cycle of signal, the power amplifier is known as **class A power amplifier**.
- **Class B Power amplifier** − When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.

- **Class C Power amplifier** − When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**.

- The class A power amplifier as discussed in the previous chapter, is the circuit in which the output current flows for the entire cycle of the AC input supply. We also have learnt about the disadvantages it has such as low output power and efficiency. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

  TRANSFORMER COUPLED CLASS A POWER AMPLIFIER

- The **construction of class A power amplifier** can be understood with the help of below figure. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.



Here R_1 and R_2 provide potential divider arrangement. The resistor Re provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer.

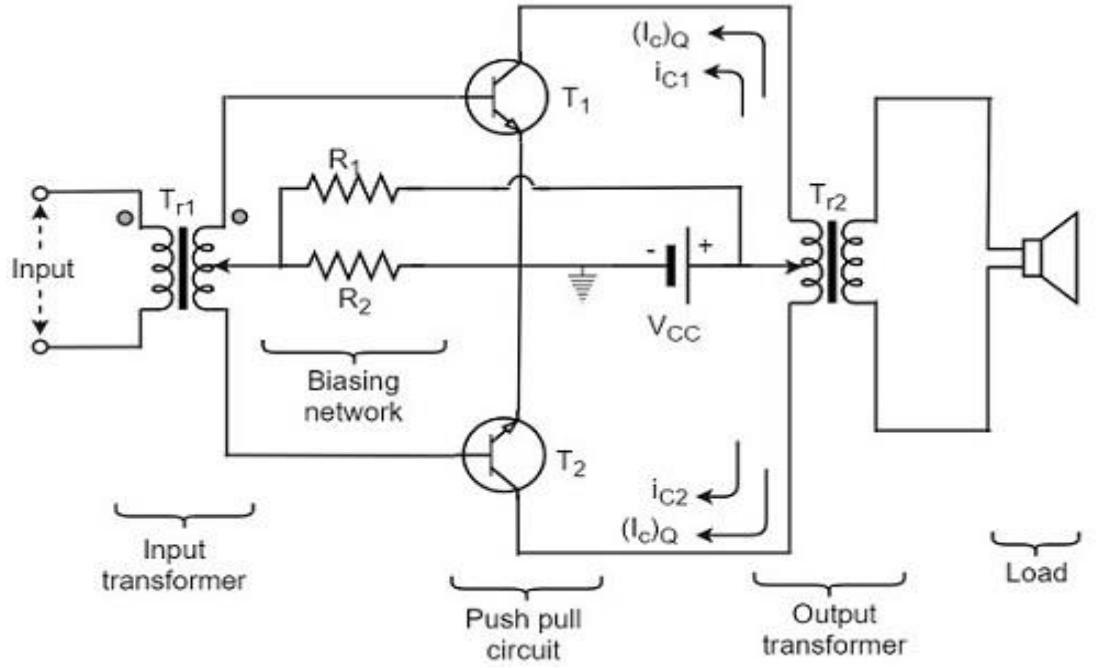
The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Class a push pull amplifier

In this circuit, we use two complementary transistors in the output stage with one transistor being an NPN or N-channel type while the other transistor is a PNP or P-channel (the complement) type connected in order to operate them like **PUSH a transistor to ON** and **PULL another transistor to OFF** at the same time. This push-pull configuration can be made in class A, class B, class C or class AB amplifiers

Construction of Push-Pull Class A Power Amplifier

The construction of the class A power amplifier circuit in push-pull configuration is shown as in the figure below. This arrangement mainly reduces the harmonic distortion introduced by the non-linearity of the transfer characteristics of a single transistor amplifier.



In Push-pull arrangement, the two identical transistors T_1 and T_2 have their emitter terminals shorted. The input signal is applied to the transistors through the transformer T_{r1} which provides opposite polarity signals to both the transistor bases. The collectors of both the transistors are connected to the primary of output transformer T_{r2}. Both the transformers are center tapped. The V_{cc} supply is provided to the collectors of both the transistors through the primary of the output transformer.

The resistors R_1 and R_2 provide the biasing arrangement. The load is generally a loudspeaker which is connected across the secondary of the output transformer. The turns ratio of the output transformer is chosen in such a way that the load is well matched with the output impedance of the transistor. So maximum power is delivered to the load by the amplifier.

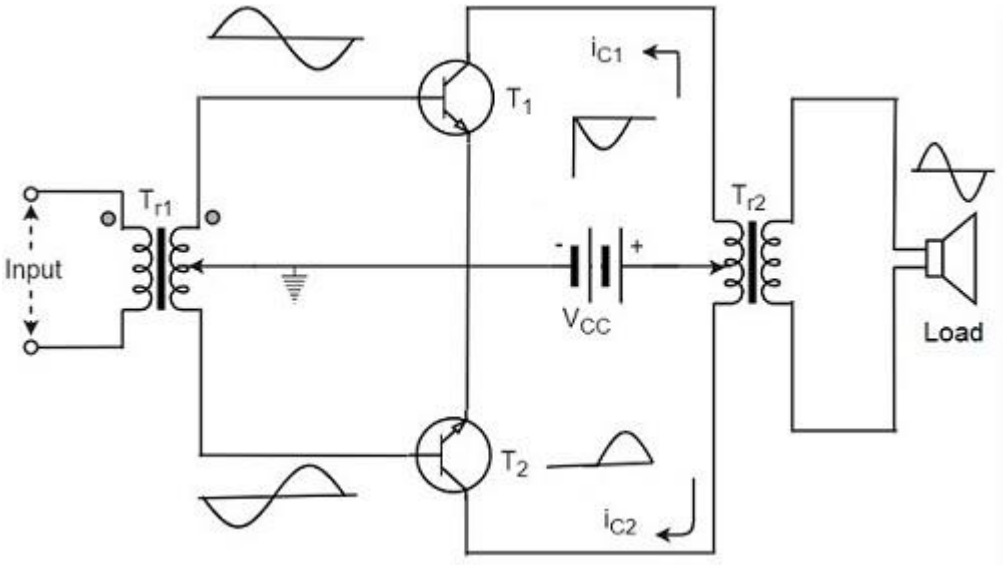
Class B Push-Pull Amplifier

Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction

The circuit of a push-pull class B power amplifier consists of two identical transistors T_1 and T_2 whose bases are connected to the secondary of the center-tapped input transformer T_{r1}. The emitters are shorted and the collectors are given the V_{cc} supply through the primary of the output transformer T_{r2}.

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.



Operation

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As no current is drawn from V_{cc}, no power is wasted.

When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180° out of phase with each other. These two signals are given to the two identical transistors T_1 and T_2. For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cutoff condition and hence no collector current flows

CHAPTER-7

FIELDEFFECT TRANSISTORS

Field-Effect Transistors

INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. JFET transistor is a voltage-controlled device. For the FET the current I_D will be a function of the voltage V_{GS} applied to the input circuit. The FET is a unipolar device depending solely on either electron (n- channel) or hole (p -channel) conduction.

The term field effect in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

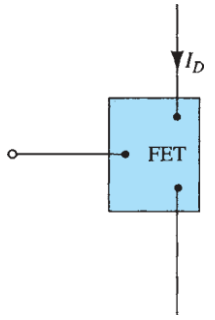


FIG. 1
voltage-controlled amplifiers.

Comparison of some of the general characteristics of BJT with FET:

One of the most important characteristics of the FET is its high input impedance.

The variation in output current is typically a great deal more for BJTs than for FETs for the same change in the applied voltage.

FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Type of FET:

Three types of FETs : the junction field-effect transistor (JFET), the metal–oxide–semiconductor field-effect transistor (MOSFET), and the metal– semiconductor field-effect transistor (MESFET). The MOSFET category is further broken down into depletion and enhancement types. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

CONSTRUCTION AND CHARACTERISTICS OF JFETs

JFET is a three-terminal device with one terminal capable of controlling the current between the other two. The major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. In the absence of any applied potentials the JFET has two *p*–*n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 2 that resembles the same region of a diode under no-bias conditions.

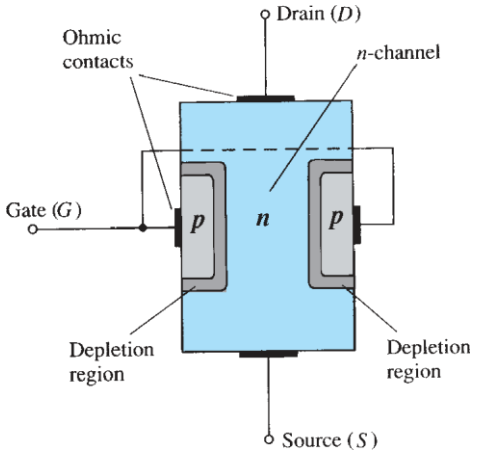


FIG. 2
Junction field-effect transistor (JFET).

V_G = 0 V, V_{DS} Some Positive Value

A positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition V_{GS} =0 V .Under the conditions the flow of charge is relatively uninhibited and is limited solely by the resistance of the n-channel between drain and source. The depletion region is wider near the top of both type materials. The current I_D will establish the voltage levels through the channel as indicated on the figure. The result is that the upper region of the p-type material will be reverse-biased by about.

As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS}.As V_{DS} increases and approaches a level referred to as V_P , the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would touch" , a condition referred to as pinch-off will result.

FIG 3 JFET at V_{GS} = 0 V and V_{DS} 7 0 V

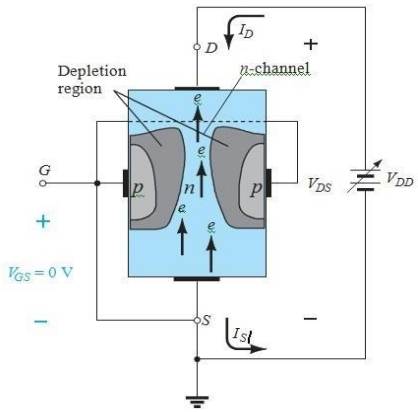
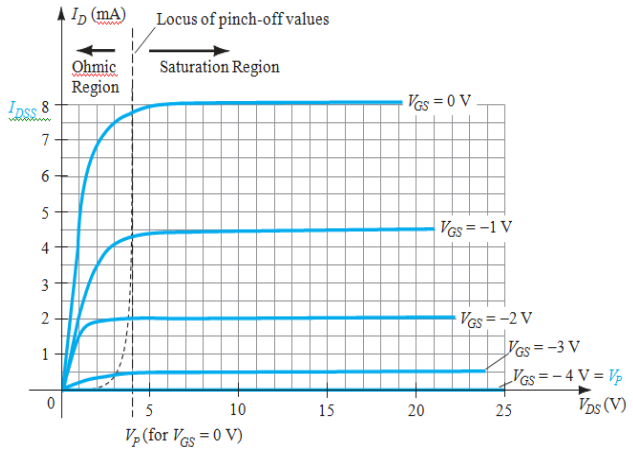


FIG 4 ID versus VDS for VGS = 0 V.



As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions increases in length long the channel, but the level of I_D remains essentially the same. In essence, therefore, once V_{DS} 7 V_P the JFET has the characteristics of a current source. As shown in Fig. 5, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels 7 V_P) is determined by the applied load.

The choice of notation I_{DSS} is derived from the fact that it is the drain-to-source current with a short circuit connection from gate to source.I_{DSS} is the maximum drain current for a JFET and is defined by the conditions V_{GS} =0 V and

V_{DS}>| VP |.

VGS < 0 V

The voltage from gate to source, denoted *VGS*, is the controlling voltage of the JFET. Curves of *ID* versus *VDS* for various levels of *VGS* can be developed for the JFET. For the *n*-channel device the controlling voltage *VGS* is made more and more negative from its *VGS*= 0 V level. The effect of the applied negative-bias *VGS* is to establish depletion regions similar to those obtained with *VGS* 0 V, but at lower levels of *VDS*. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of *VDS*, as shown in Fig. 6 for *VGS* = – 1 V. The resulting saturation level for *ID* has been reduced and in fact will continue to decrease as *VGS* is made more and more negative. Eventually, *VGS* when *VGS* = – *VP* will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

The level of VGS that results in ID= 0 mA is defined by VGS =VP, with VP being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

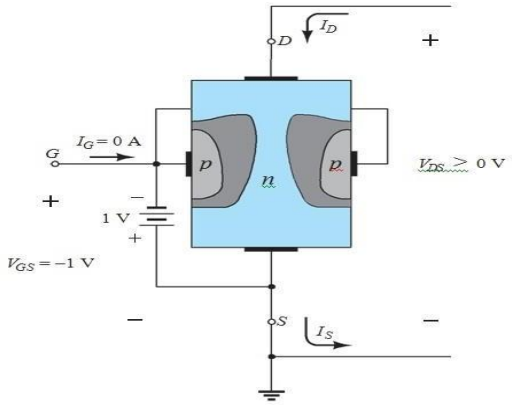


FIG.5

FIG. 6

Application of a negative voltage to the gate of a JFET. *n-Channel JFET characteristics with IDSS = 8 mA and VP = -4 V.*

TRANSFER CHARACTERISTICS

Derivation

For the BJT transistor the output I_C current and the input controlling I_B current are related by beta, which was considered constant for the analysis to be performed. In equation form

$$I_C = f(I_B) = \beta I_B \quad -(1)$$

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad -(2)$$

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed

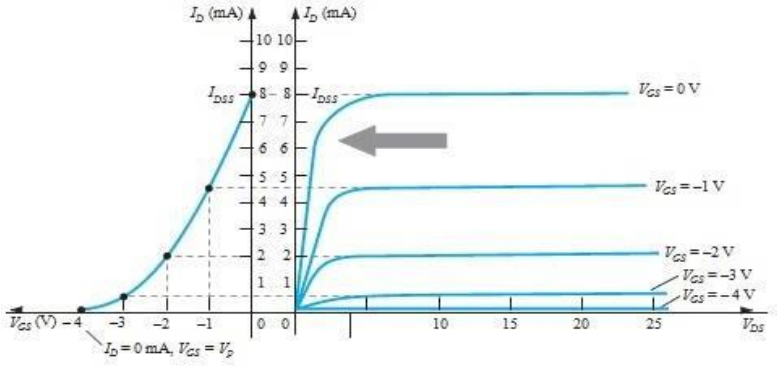
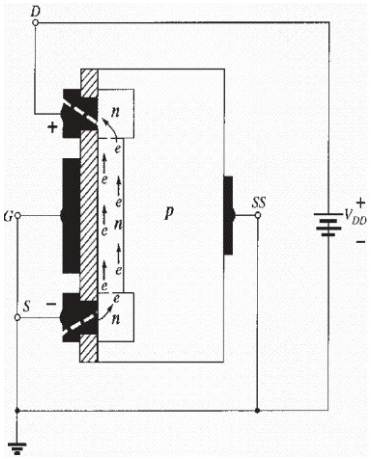


FIG.7 Obtaining the transfer curve from the drain characteristics.

DEPLETION-TYPE MOSFET

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation; the name MOSFET stands for metal–oxide–semiconductor field-effect transistor



Basic Construction:

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a dielectric, which sets up opposing (as indicated by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

Basic Operation:

The gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals. The result is an attraction of the free electrons of the n-channel for the positive voltage at the drain. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with V_{GS} 0 V continues to be labeled I_{DSS}.

V_{GS} is set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract).

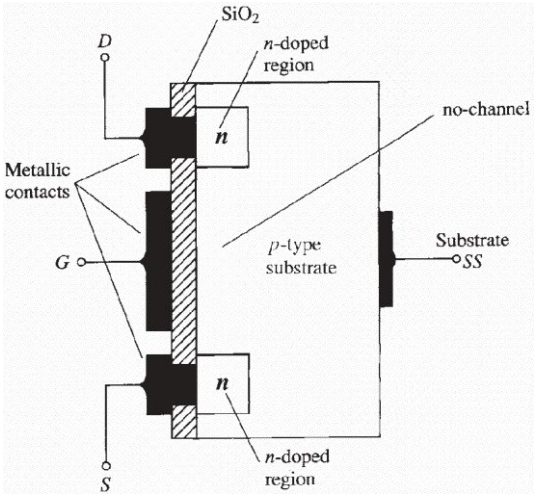
Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

ENHANCEMENT-TYPE MOSFET

The characteristics of the enhancement-type MOSFET are quite different from depletion type MOSFET.

Basic Construction:

A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead (labeled SS) is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to n-doped regions, but note in Fig. the absence of a channel between the two n-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.



Basic Operation:

If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device of Fig, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the n-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p–n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

The level of V_{GS} that results in the significant increase in drain current is called the threshold voltage and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with V_{GS} 0 V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET.

FET Biasing

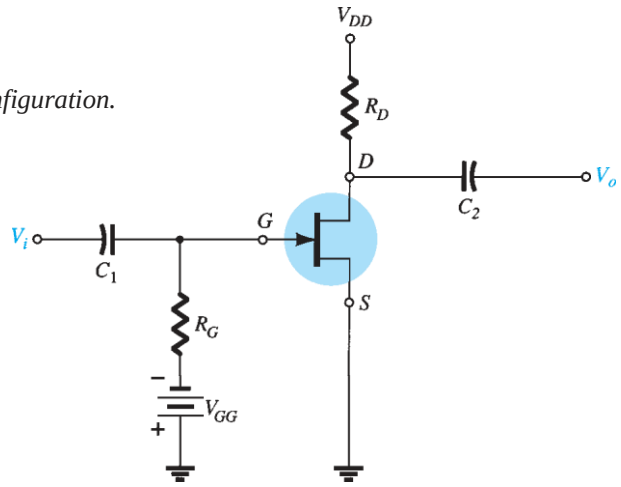
For the field-effect transistor, the relationship between input and output quantities is nonlinear due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

FIXED-BIAS CONFIGURATION:

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig.1. Referred to as the fixed-bias configuration,

FIG. 1

Fixed-bias configuration.



For the dc analysis, $V_{RG} = I_G R_G = (0\text{ A})R_G = 0\text{ V}, \quad I_G \cong 0\text{ A}$

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction results in

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

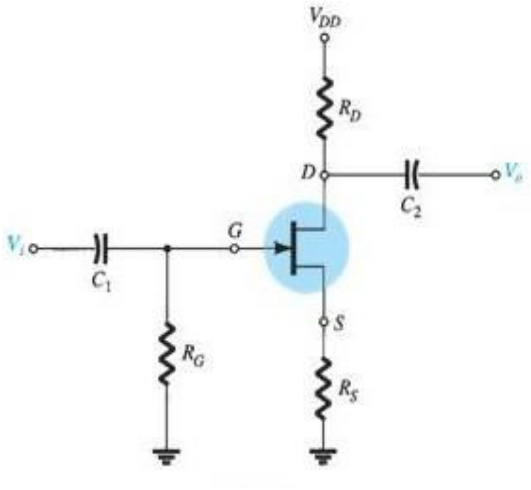
The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$V_{DS} = V_{DD} - I_D R_D$$

$= V_{DS} + = V_{DS} + 0\text{ V},$

$V_D = V_{DS}, V_G = V_{GS}$

SELF-BIAS CONFIGURATION



The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A.

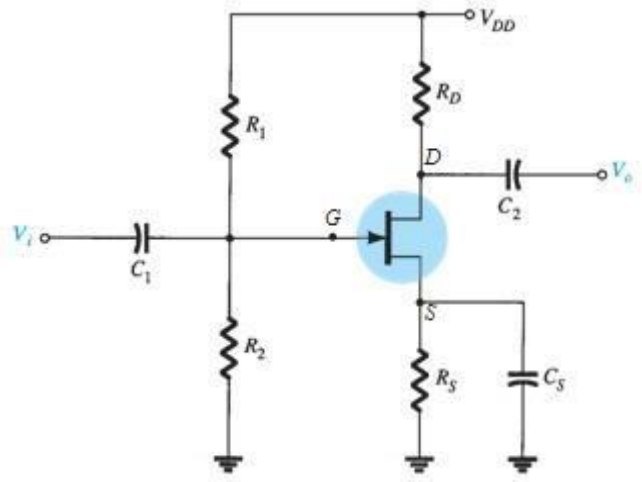
The current through R_S is the source current I_S, but $I_S = I_D$ and $V_{R_S} = I_D R_S$

$$V_{GS} = -I_D R_S$$

that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

VOLTAGE-DIVIDER BIASING

The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and volt- age in both the input and output circuits. Recall that I_B provides the link between input and output circuits for the BJT voltage-divider configuration, whereas V_{GS} does the same for the FET configuration.



Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R1} = I_{R2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law

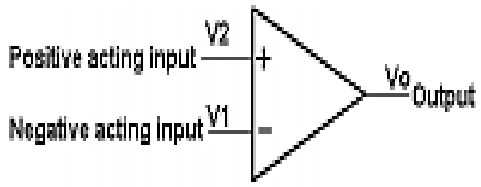
$$V_{GS} = V_G - I_D R_S$$

CHAPTER-8

OPERATIONAL AMPLIFIER

Operational Amplifier

The Operational Amplifier is a direct-coupled , high gain , negative feedback amplifier. It is nothing more than a differential amplifier which amplifies the difference between two inputs.



General circuit diagram of an op-amp

The terminal marked - is called the inverting terminal which means signal applied there will appear phase inverted at the output while the terminal marked + is called the non inverting terminal means that the signal applied here will appear in phase and applied at the output . Please understand that the - and + do not denote any type of voltage it means that output voltage is proportional to the difference of Non Inverting and inverting voltages which is **Vo = V2 - V1** . When there is no feedback , no voltage or capacitor between output and input the op-amp is said to be in open loop condition .

Characteristics of an ideal op-amp

An Ideal Op-Amp has the following characteristics.

* An infinite voltage gain
* An infinite bandwidth
* An infinite input resistance: The resistance b/w V1 and V2 terminals is infinite .
* Zero output resistance: Vo remains constant no matter what resistance is applied across output .
* Perfect balance: When V1 is equal to V2 the Vo is 0 .

Single-Ended Input

Single-ended input operation results when the input signal is connected to one inputwith the other input connected to ground**.**

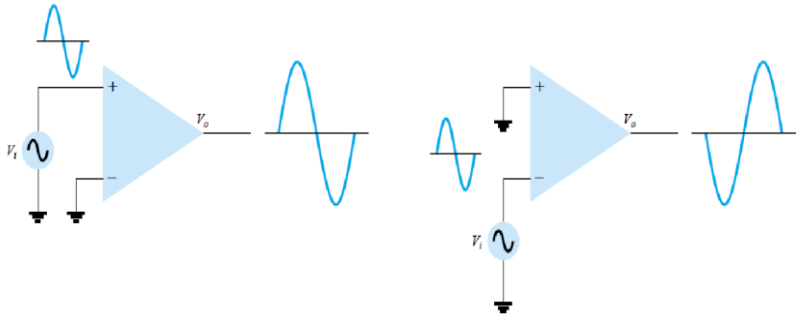


FIG.2.Single ended input

Double-Ended Output

While the operation discussed so far had a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 1. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 3 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 4 shows the same operation with a single output measured.

FIG.3Double-ended output

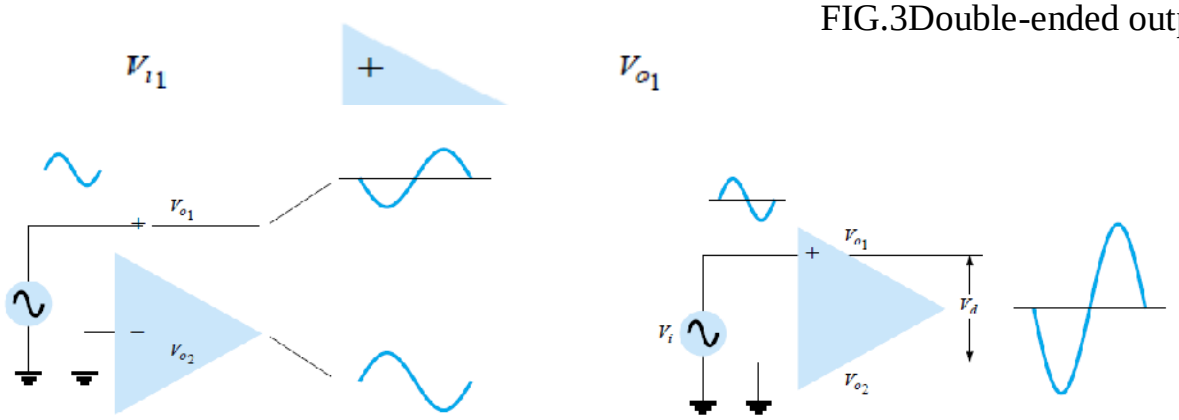


FIG.4Double-ended output with single-ended input

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, the two inputs are equally amplified, and since they result in opposite polarity signals at the output, these signals cancel, resulting in0-V output. Practically, a small output signal will result

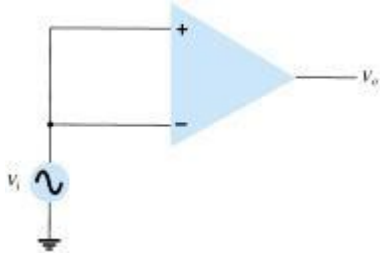


FIG.5Common-modeoperation

Common-Mode Rejection

A significant feature of a differential connection is that the signals which are opposite at the inputs are highly amplified, while those which are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs.

DIFFERENTIAL AND COMMONMODEOPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs**.**

$$V_d = V_{i_1} - V_{i_2}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputscan be defined as the average of the sum of the two signals.

$$V_c = \frac{1}{2}(V_{i_1} + V_{i_2})$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of phase components, the resulting output can be expressed as

$$V_o = A_d V_d + A_c V_c$$

Where *Vd* = difference voltage given by Eq.
Vc = common voltage given by Eq.
Ad =differential gain of the amplifier
Ac = common-mode gain of the amplifier

Common-Mode Rejection Ratio

Having obtained *Ad* and *Ac* (as in the measurement procedure discussed above), wecan now calculate a value for the common-mode rejection ratio (CMRR), which isdefined by the following equation:

$$\text{CMRR} - \frac{A_d}{A_c}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} \quad \text{(dB)}$$

We can express the output voltage in terms of the value of CMRR as follows:

$$V_o = A_d V_d + A_c V_c = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

$$V_o = A_d V_d \left(1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d}\right)$$

Basic of Op-Amp

The circuit shown provides operation as a constant-gain multiplier. An input signal, *V*1, is applied through resistor *R*1 to the minus input. The output is then connected back to the same minus input through resistor *Rf*. The plus input is connected to ground. Since the signal *V*1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 6a shows the op-amp replaced by its ac equivalent
circuit. If we use the ideal op-amp equivalent circuit, replacing *Ri* by an infinite resistance and *Ro* by zero resistance, the ac equivalent circuit is that shown in Fig.6b. The circuit is then redrawn, as shown in Fig. 6c, from which circuit analysis is carried out.

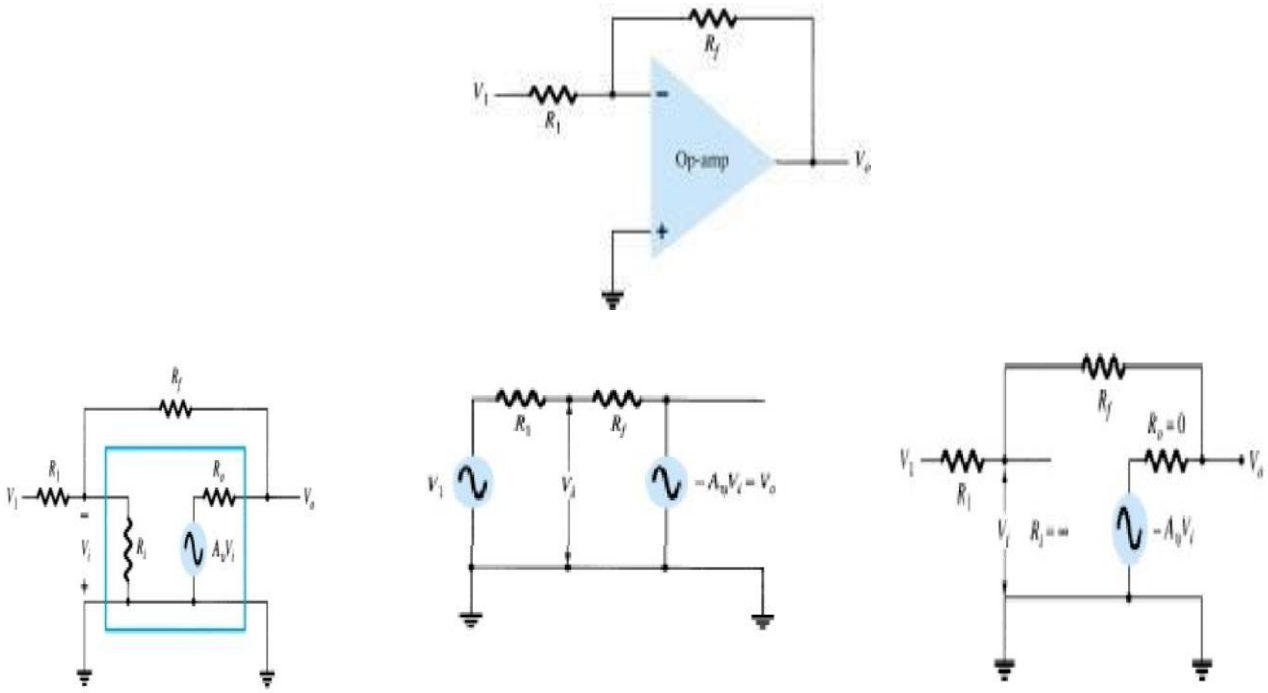


FIG.6.Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

Using superposition, we can solve for the voltage V_1 in terms of the components due to each of the sources. For source V_1 only ($-A_vV_i$ set to zero),

$$V_{i_1} = \frac{R_f}{R_1 + R_f} V_1$$

For source $-A_vV_i$ only (V_1 set to zero),

$$V_{i_2} = \frac{R_1}{R_1 + R_f} (-A_vV_i)$$

The total voltage V_i is then

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f} V_1 + \frac{R_1}{R_1 + R_f} (-A_vV_i)$$

which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1} V_1$$

If $A_v \gg 1$ and $A_v R_1 \gg R_f$, as is usually true, then

$$V_i = \frac{R_f}{A_vR_1} V_1$$

Solving for V_o/V_i, we get

$$\frac{V_o}{V_i} = \frac{-A_vV_i}{V_i} = \frac{-A_v}{V_i} \frac{R_fV_1}{A_vR_1} = -\frac{R_f}{R_1} \frac{V_1}{V_i}$$

$$\boxed{\frac{V_o}{V_1} = -\frac{R_f}{R_1}}$$

Unity Gain

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

If $R_f = R_1$, the

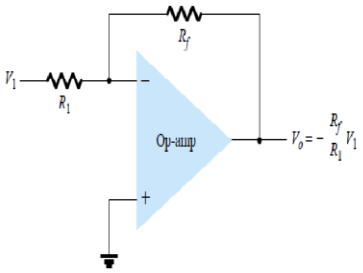
$$\boxed{\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}}$$

so that the circu
actly R_1, the vo

PRACTICAL OP-AMP CIRCUITS

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (*R*1) and feedback resistor (*Rf*)—this output also being inverted from the input. Using Eq. (14.8) we can write



$$V_o = -\frac{R_f}{R_1} V_1$$

Noninverting Amplifier

The connection of Fig. 8shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 14.16b. Note that the voltage across *R*1 is *V*1 since *Vi* =0 V. This must be equal to the output voltage, through a voltage divider of *R*1 and *Rf*, so that

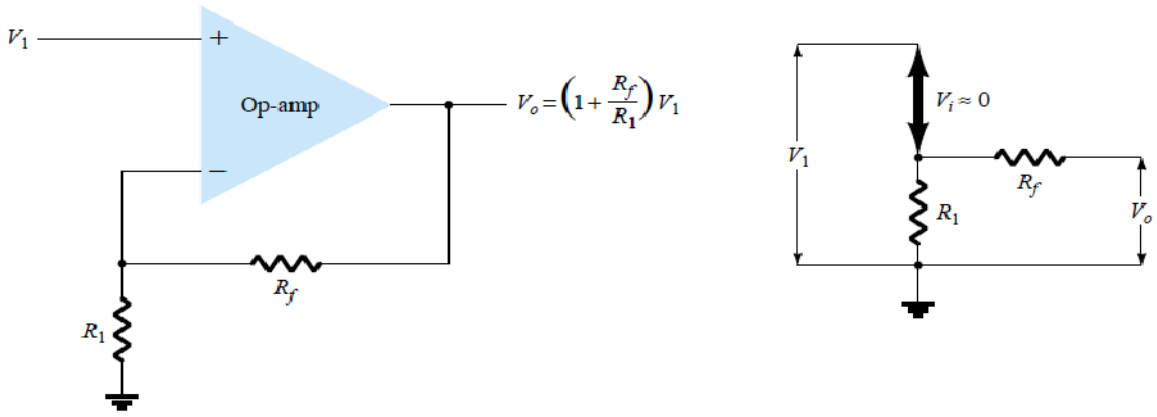


FIG.8.Noninverting constant-gain multiplier

Summing amplifier

The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor. Using the equivalent representation shown in Fig. 9, the output voltage can be expressed in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

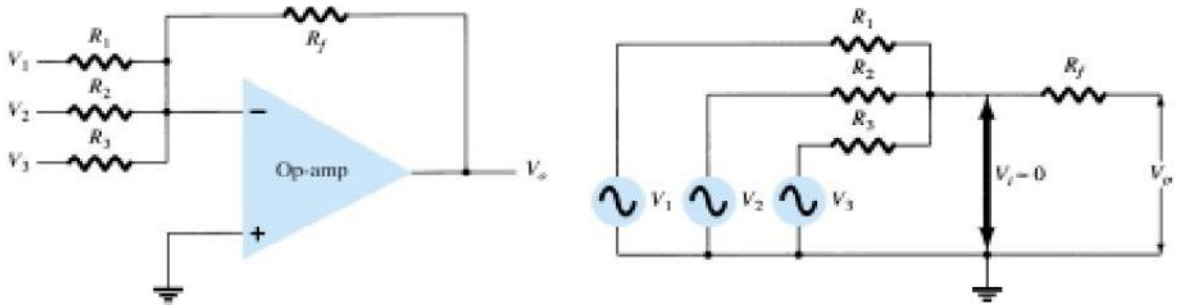


FIG.9Summing amplifier; (b) virtual-ground equivalent circuit.

Subtractor:

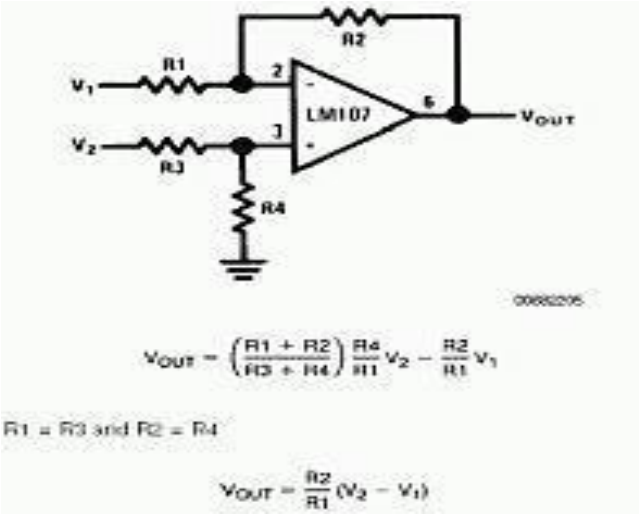


FIG.10 Substractor

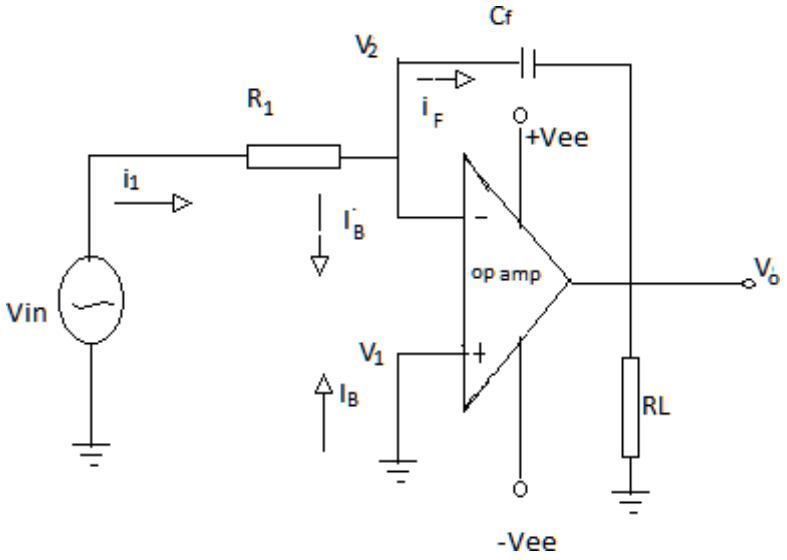
The aim of the subtractor is to provide an output which is equal to the difference of the two input signals or proportional to their difference. For minimum offset error R1 || R2 = R3 || R4 .

Op-Amp as Integrator

The operational amplifier integrator is an electronic integration circuit. Based around the operational amplifier (op-amp), it performs the mathematical operation of integration with respect to time; that is, its output voltage is proportional to the input voltage integrated over time.

The input current is offset by a negative feedback current flowing in the capacitor, which is generated by an increase in output voltage of the amplifier. The output voltage is therefore dependent on the value of input current it has to offset and the inverse of the value of the feedback capacitor. The greater the capacitor value, the less output voltage has to be generated to produce a particular feedback current flow.

Ideal circuit



The circuit operates by passing a current that charges or discharges the capacitor C_f during the time under consideration, which strives to retain the virtual ground condition at the input by off-setting the effect of the input current. Referring to the above diagram, if the op-amp is assumed to be ideal, nodes v_1 and v_2 are held equal, and so v_2 is a virtual ground. The input voltage passes a current v_{in}/R_1.through the resistor producing a compensating current flow through the series capacitor to maintain the virtual ground. This charges or discharges the capacitor over time. Because the resistor and capacitor are connected to a virtual ground, the input current does not vary with capacitor charge and a linear integration of output is achieved.

The circuit can be analyzed by applying Kirchhoff's current law at the node v_2, keeping ideal op-amp behavior in mind.

$$i_1 = I_B + i_F$$

$I_B = 0$ in an ideal op-amp, so:

$$i_1 = i_F$$

Furthermore, the capacitor has a voltage-current relationship governed by the equation:

$$I_C = C\frac{dV_c}{dt}$$

Substituting the appropriate variables:

$$\frac{v_{in} - v_2}{R_1} = C_F\frac{d(v_2 - v_o)}{dt}$$

$v_2 = v_1 = 0$ in an ideal op-amp, resulting in:

$$\frac{v_{in}}{R_1} = -C_F\frac{dv_o}{dt}$$

Integrating both sides with respect to time:

$$\int_0^t \frac{v_{in}}{R_1}\,dt = -\int_0^t C_F\frac{dv_o}{dt}\,dt$$

If the initial value of v_o is assumed to be 0 V, this results in a DC error of:

$$v_o = -\frac{1}{R_1 C_F}\int_0^t v_{in}\,dt$$

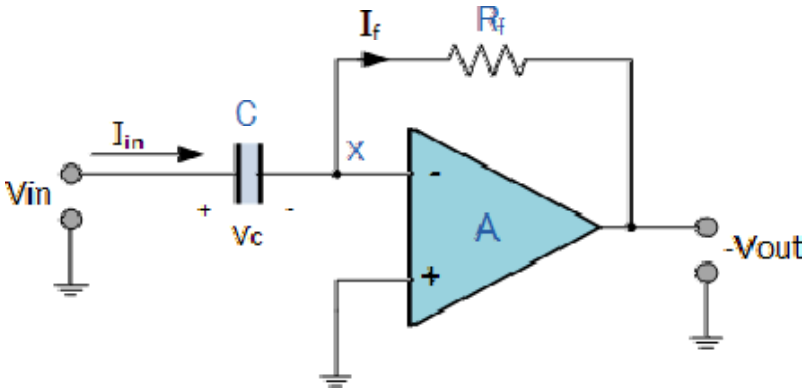
The Op-amp Differentiator Amplifier

The basic **Op-amp Differentiator** circuit is the exact opposite to that of the Integrator Amplifier circuit that we looked at in the previous tutorial. Here, the position of the capacitor and resistor have been reversed and now the reactance, Xc is connected to the input terminal of the inverting amplifier while the resistor, R*f* forms the negative feedback element across the operational amplifier as normal.

This Operational Amplifier circuit performs the mathematical operation of **Differentiation** that is it "*produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time*". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

As with the integrator circuit, we have a resistor and capacitor forming an RC Network across the operational amplifier and the reactance (Xc) of the capacitor plays a major role in the performance of a **Op-amp Differentiator**.

Op-amp Differentiator Circuit



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R*f*/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R*f*.

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C\,\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore\ -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C\,\frac{dV_{IN}}{dt}$$

Therefore, the output voltage Vout is a constant -R*f*.C times the derivative of the input voltage Vin with respect to time. The minus sign indicates a 180^o phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.